Republic of Iraq

Ministry of Higher Education and Seintific Reserch University of AL-Anbar

College of Engineering

Electrical Engineering Department

Electronic I

By

Hatem Fahd Al-Duliamy

2018-2019

UNIVERSITY OF ANBAR

COLLEGE OF ENGINEERING

ELECTRICAL ENGINEERING DEPARTMENT

Electronic I

Third Class

Chapter 09

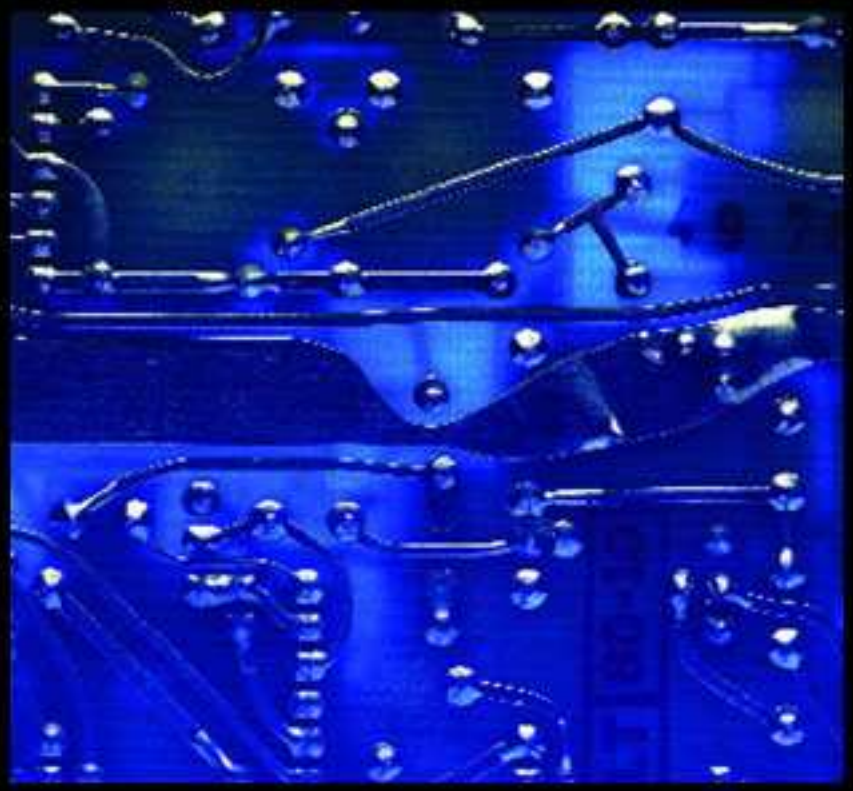
Ch09_ BJT and JFET Frequency Response

Hatem Fahd Al-Duliamy

2018-2019

ELECTRONIC DEVICES AND CIRCUIT THEORY

TENTH EDITION



BOYLESTAD

PEARSON

Chapter 9: BJT and JFET Frequency Response

Hatem Fahd Al-Duliamy

CHAPTER OBJECTIVES:

- Develop confidence in the use of logarithms, understand the concept of decibels, and be able to accurately read a logarithmic plot
- .Become acquainted with the frequency response of a BJT and FET amplifier
- Be able to normalize a frequency plot, establish the dB plot, and find the cutoff frequencies and bandwidth
- Understand how straight-line segments and cutoff frequencies can result in a Bode plot that will define the frequency response of an amplifier
- Be able to find the Miller effect capacitance at the input and output of an amplifier due to a feedback capacitor
- Become familiar with square-wave testing to determine the frequency response of an amplifier

General Frequency Considerations

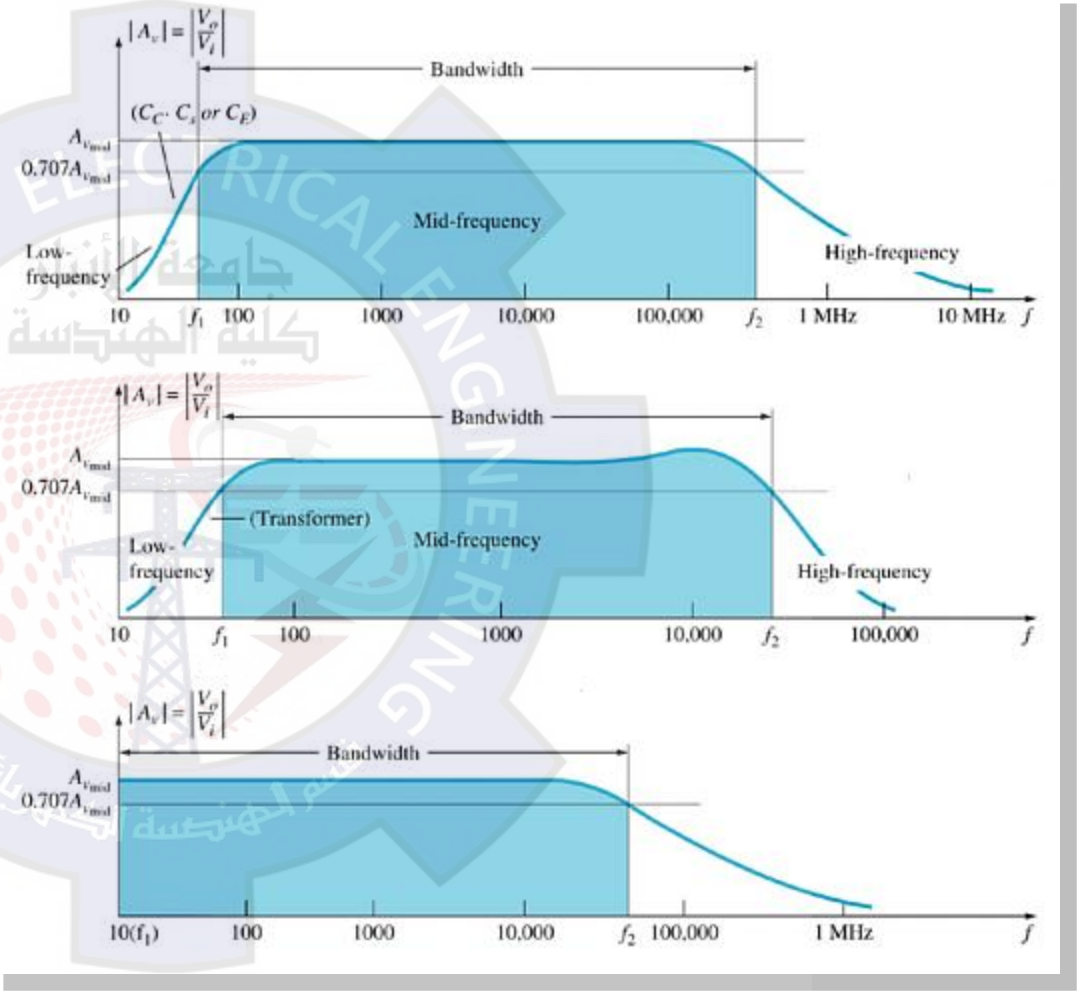
The **frequency response** of an amplifier refers to the frequency range in which the amplifier will operate with negligible effects from capacitors and device internal capacitance. This range of frequencies can be called the **mid-range**.

- At frequencies above and below the midrange, capacitance and any inductance will affect the gain of the amplifier.
- At low frequencies the coupling and bypass capacitors lower the gain.
- At high frequencies stray capacitances associated with the active device lower the gain.
- Also, cascading amplifiers limits the gain at high and low frequencies.

Bode Plot

A Bode plot indicates the frequency response of an amplifier.

The horizontal scale indicates the frequency (in Hz) and the vertical scale indicates the gain (in dB).

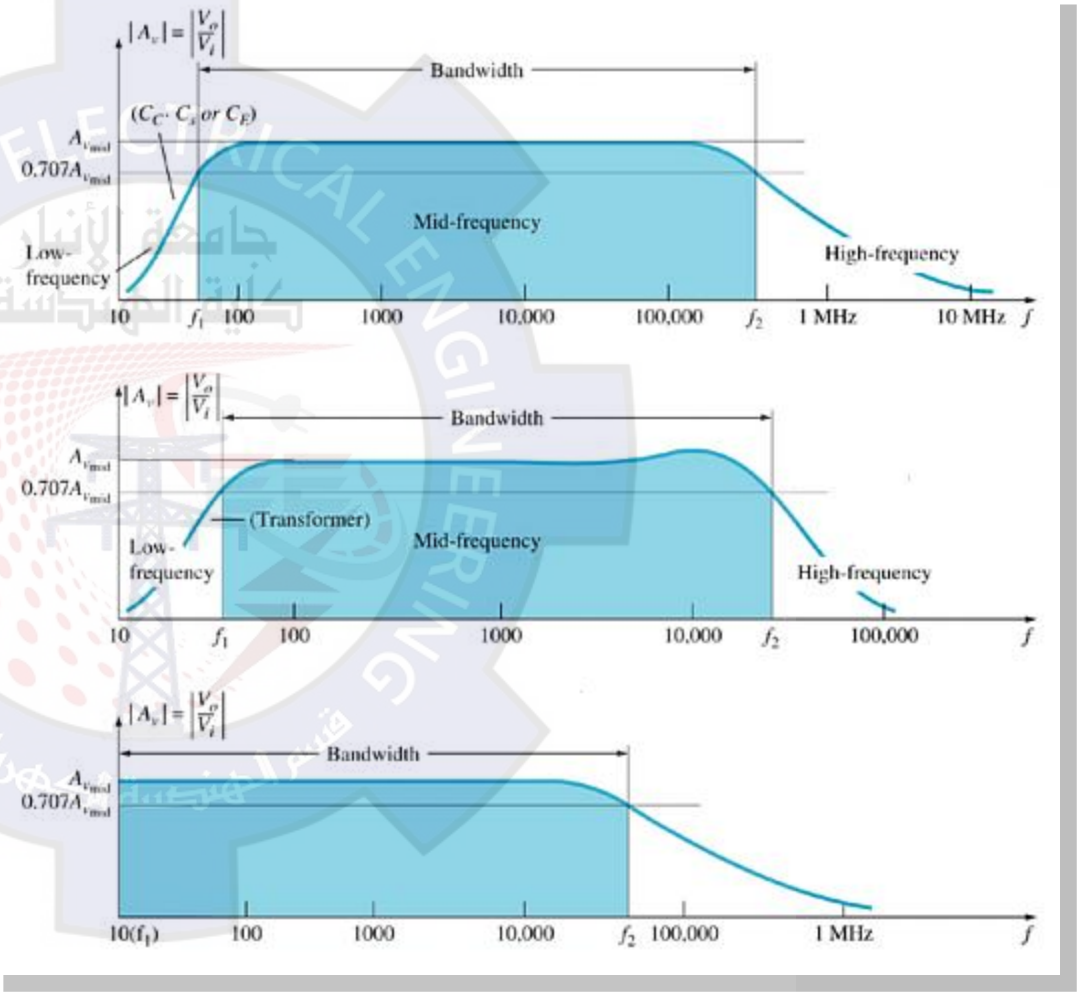


Cutoff Frequencies

The mid-range frequency range of an amplifier is called the bandwidth of the amplifier.

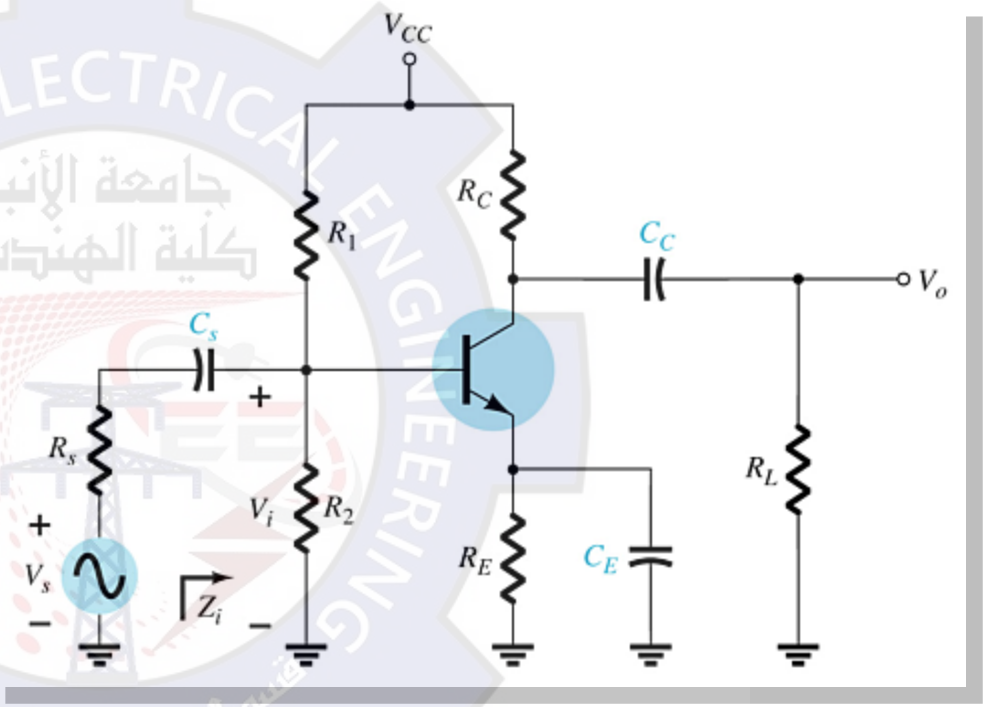
The bandwidth is defined by the lower and upper cutoff frequencies.

Cutoff – any frequency at which the gain has dropped by 3 dB.



BJT Amplifier Low-Frequency Response

At low frequencies, coupling capacitor (C_S, C_C) and bypass capacitor (C_E) reactances affect the circuit impedances.



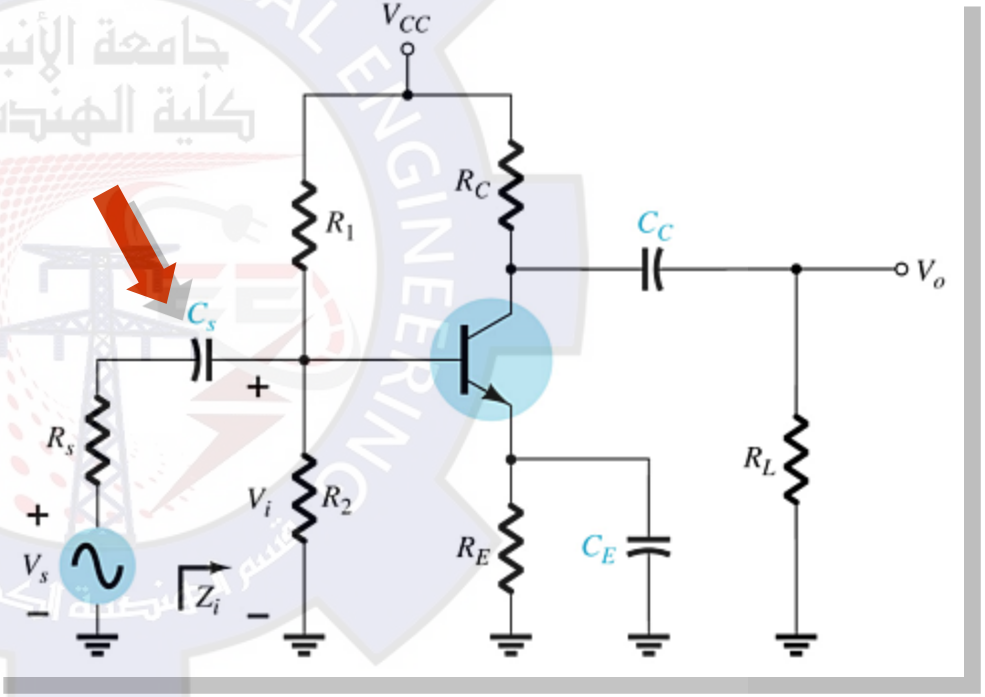
Coupling Capacitor (C_S)

The cutoff frequency due to C_S can be calculated by

$$f_{Ls} = \frac{1}{2\pi(R_s + R_i)C_s}$$

where

$$R_i = R_1 \| R_2 \| \beta r_e$$



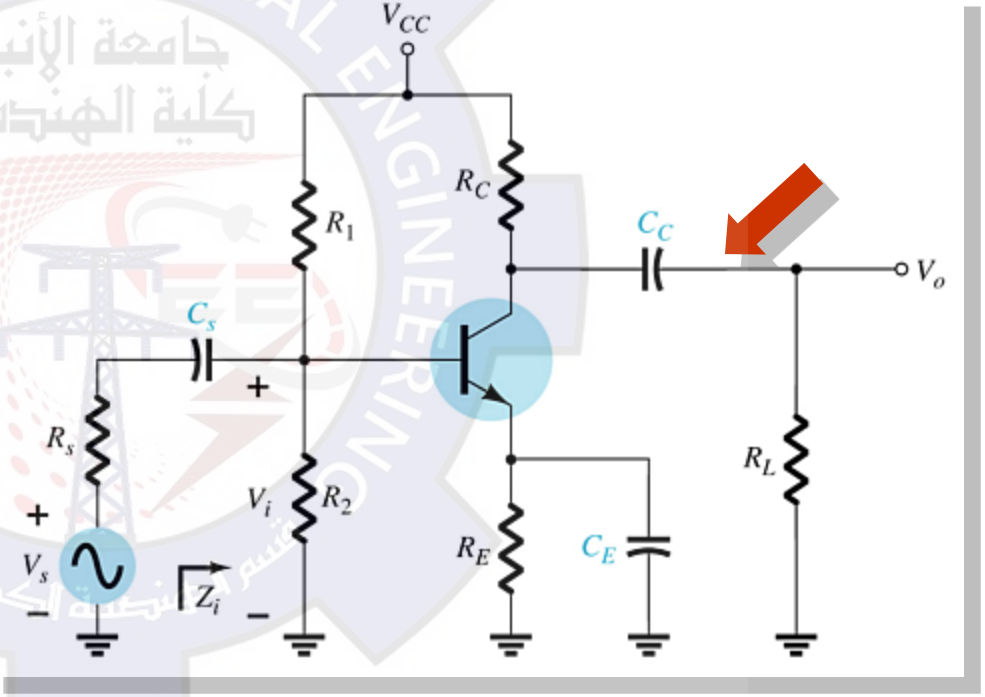
Coupling Capacitor (C_C)

The cutoff frequency due to C_C can be calculated with

$$f_{LC} = \frac{1}{2\pi(R_o + R_L)C_c}$$

where

$$R_o = R_C \,||\, r_o$$



Bypass Capacitor (C_E)

The cutoff frequency due to C_E can be calculated with

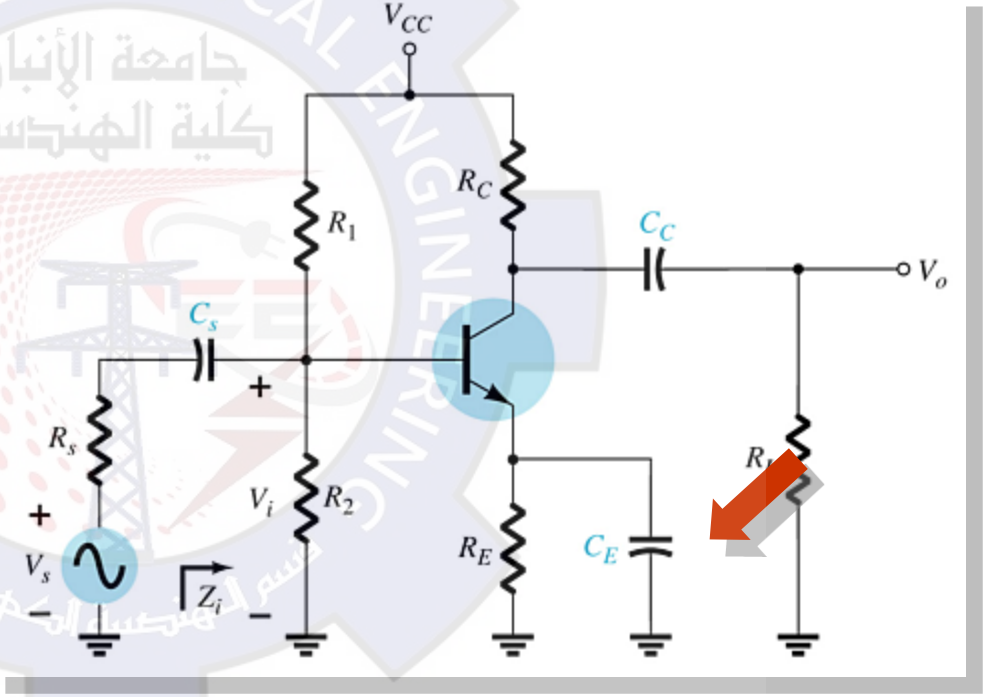
$$f_{LE} = \frac{1}{2\pi R_e C_E}$$

where

$$R_e = R_E \,||\, \left(\frac{R_s'}{\beta} + r_e\right)$$

and

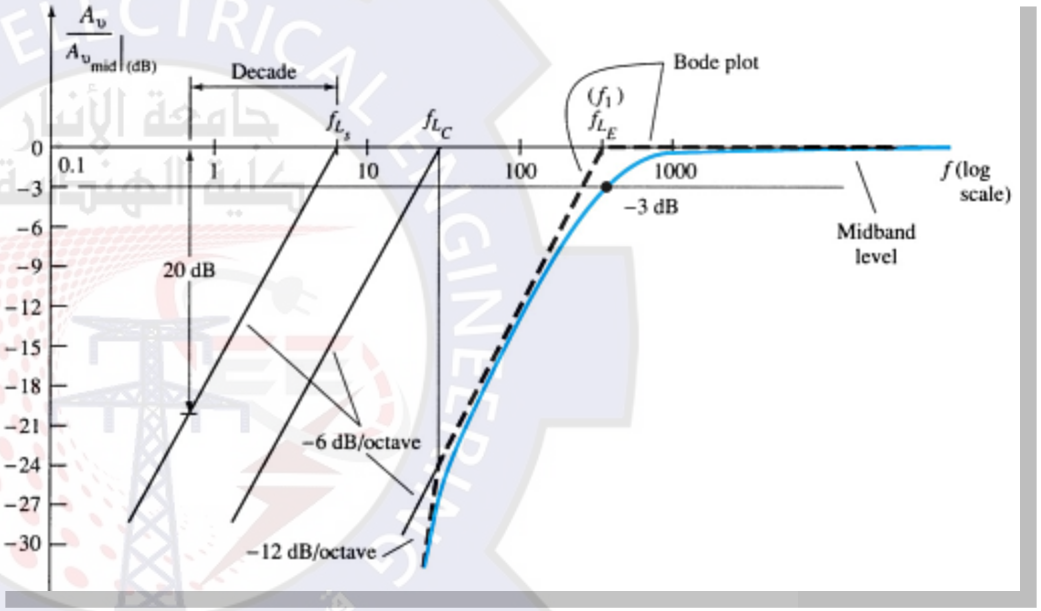
$$R_s' = R_s \,||\, R_1 \,||\, R_2$$



BJT Amplifier Low-Frequency Response

The Bode plot indicates that each capacitor may have a different cutoff frequency.

It is the device that has the *highest* lower cutoff frequency (f_L) that dominates the overall frequency response of the amplifier.

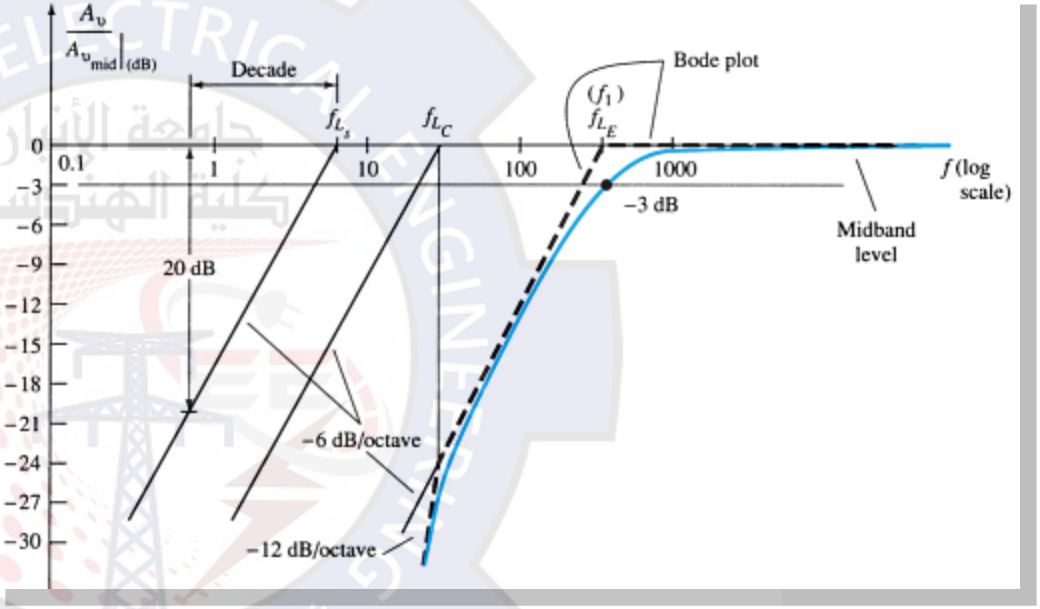


Roll-Off of Gain in the Bode Plot

The Bode plot not only indicates the cutoff frequencies of the various capacitors it also indicates the amount of attenuation (loss in gain) at these frequencies.

The amount of attenuation is sometimes referred to as roll-off.

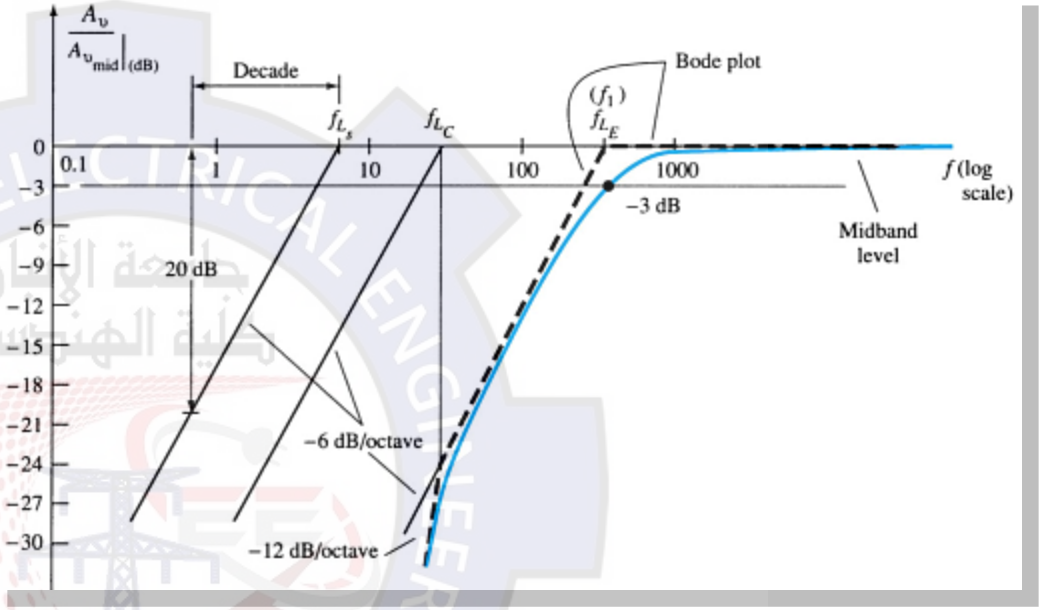
The roll-off is described as dB loss-per-octave or dB loss-per-decade.



Roll-off Rate (-dB/Decade)

-dB/decade refers to the attenuation for every 10-fold change in frequency.

For attenuations at the low-frequency end, it refers to the loss in gain from the lower cutoff frequency to a frequency that is one-tenth the cutoff value.

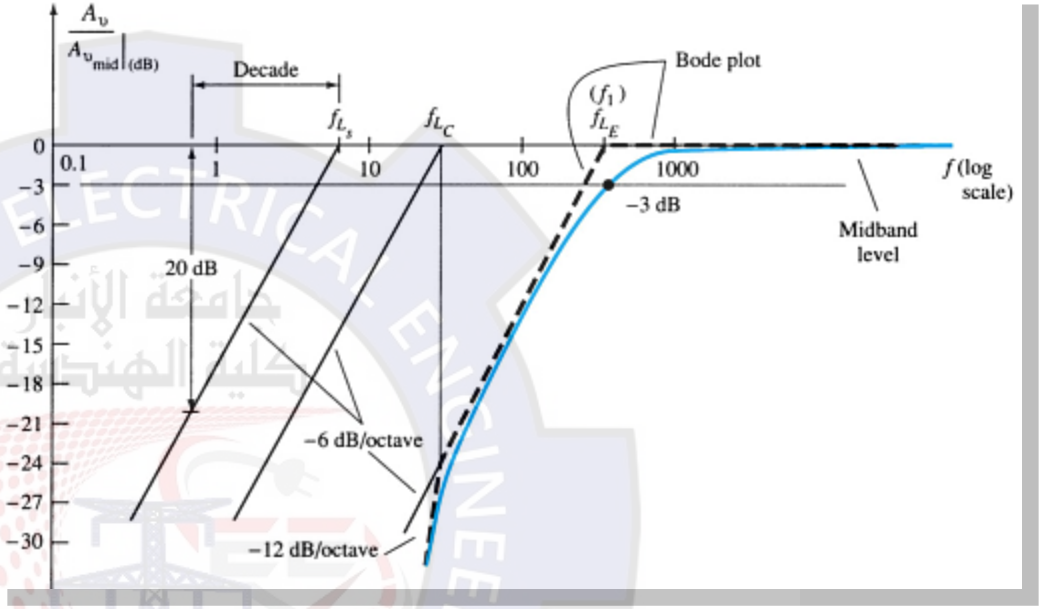


In this example:

f_{LS} = 9kHz gain is 0dB
f_{LS}/10 = .9kHz gain is –20dB
Thus the roll-off is 20dB/decade
The gain decreases by –20dB/decade

Roll-Off Rate (–dB/Octave)

-dB/octave refers to the attenuation for every 2-fold change in frequency.
For attenuations at the low-frequency end, it refers to the loss in gain from the lower cutoff frequency to a frequency one-half the cutoff value.



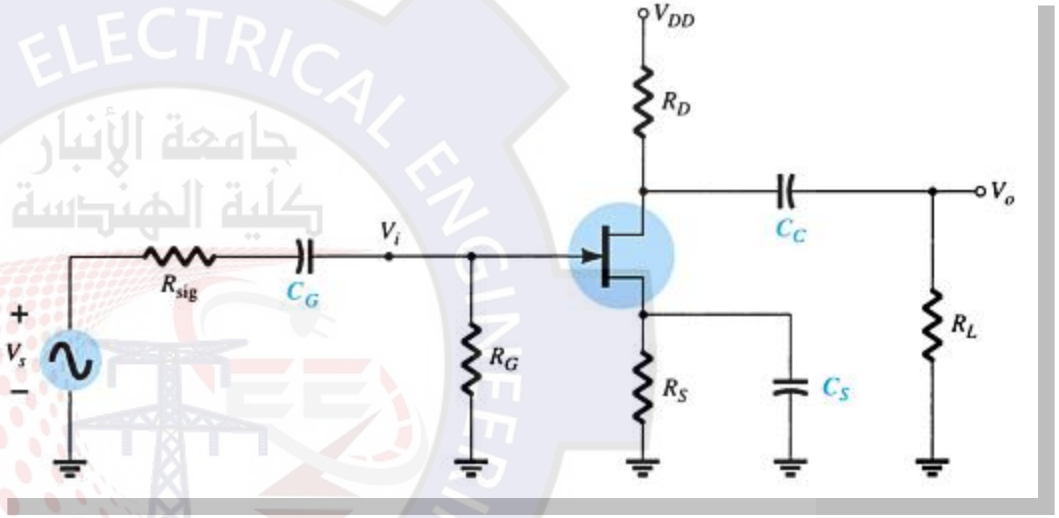
In this example:

f_{LS} = 9kHz gain is 0dB
f_{LS} / 2 = 4.5kHz gain is –6dB
Therefore the roll-off is 6dB/octave.

This is a little difficult to see on this graph because the horizontal scale is a logarithmic scale.

FET Amplifier Low-Frequency Response

At low frequencies, coupling capacitor (C_G, C_C) and bypass capacitor (C_S) reactances affect the circuit impedances.



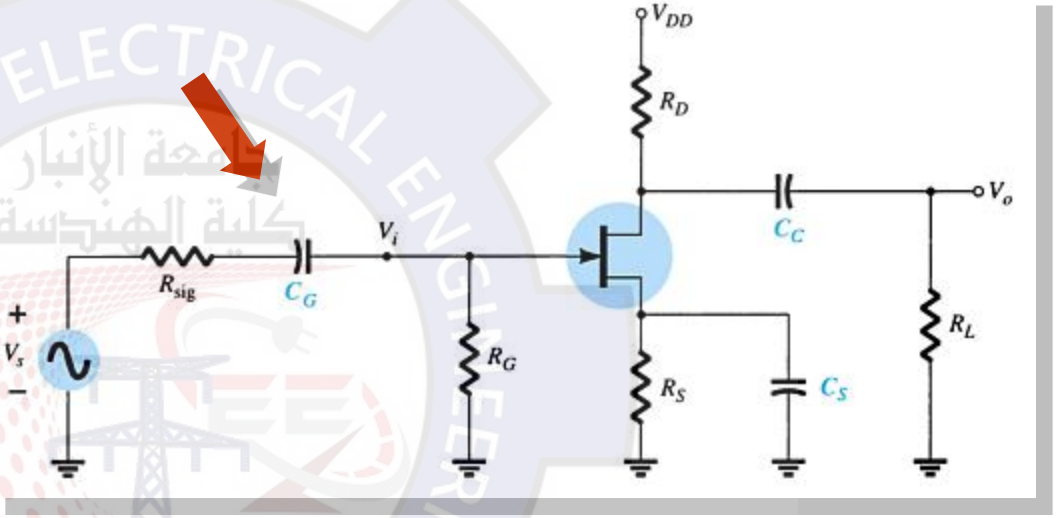
Coupling Capacitor (C_G)

The cutoff frequency due to C_G can be calculated with

$$f_{LC} = \frac{1}{2\pi(R_{sig} + R_i)C_G}$$

where

$$R_i = R_G$$



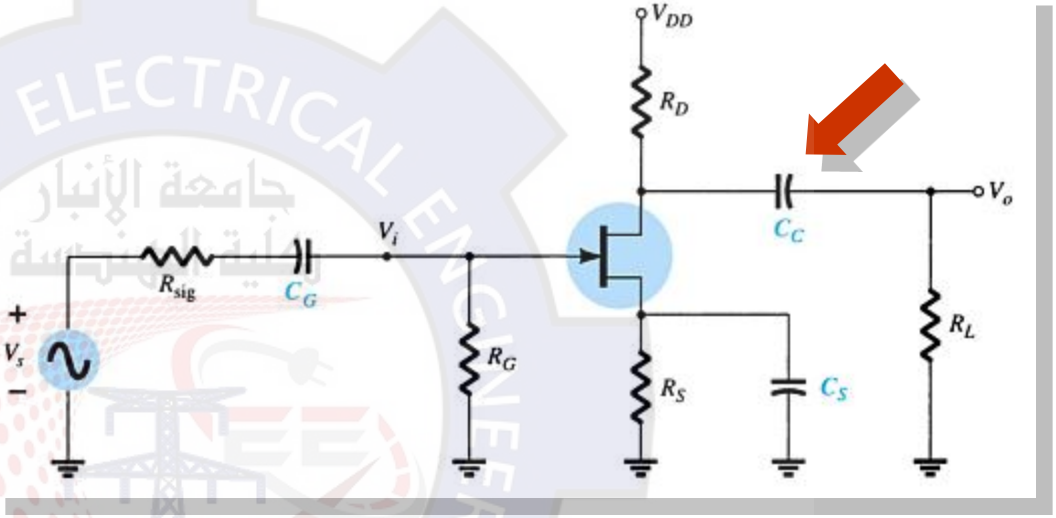
Coupling Capacitor (C_C)

The cutoff frequency due to C_C can be calculated with

$$f_{LC} = \frac{1}{2\pi(R_o + R_L)C_C}$$

where

$$R_o = R_D \| r_d$$



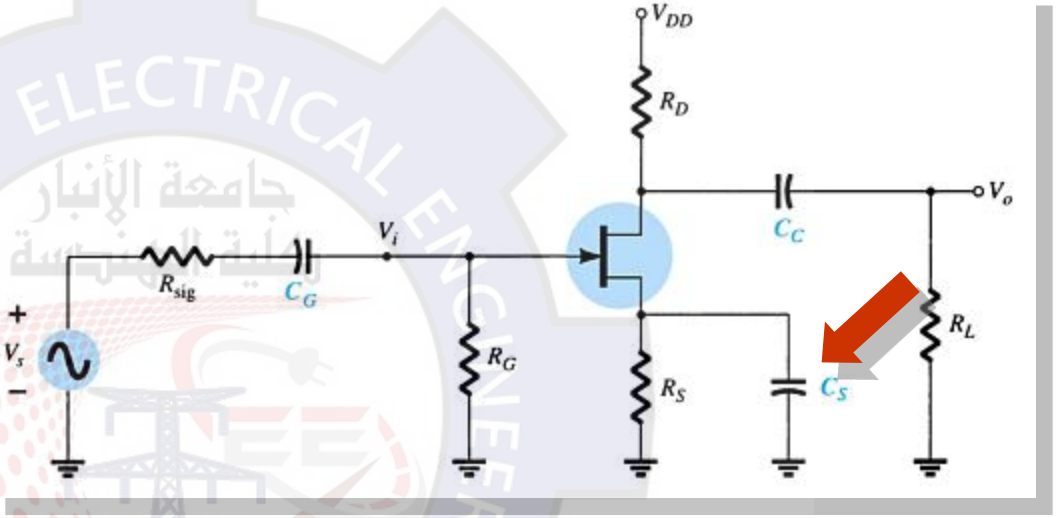
Bypass Capacitor (C_S)

The cutoff frequency due to C_S can be calculated with

$$f_{LS} = \frac{1}{2\pi R_{eq} C_S}$$

where

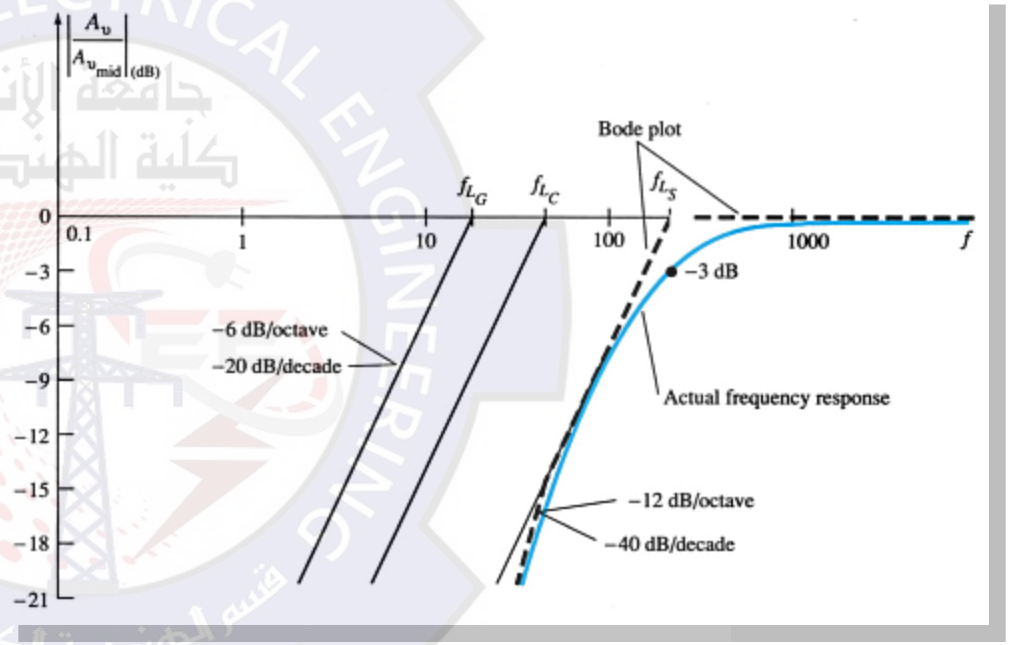
$$R_{eq} = R_S \,||\, \left|\frac{1}{g_m}\right| \, r_d \cong \infty\Omega$$



FET Amplifier Low-Frequency Response

The Bode plot indicates that each capacitor may have a different cutoff frequency.

The capacitor that has the *highest* lower cutoff frequency (f_L) is closest to the actual cutoff frequency of the amplifier.



Miller Capacitance

Any *p-n* junction can develop capacitance. In a BJT amplifier, this capacitance becomes noticeable across:

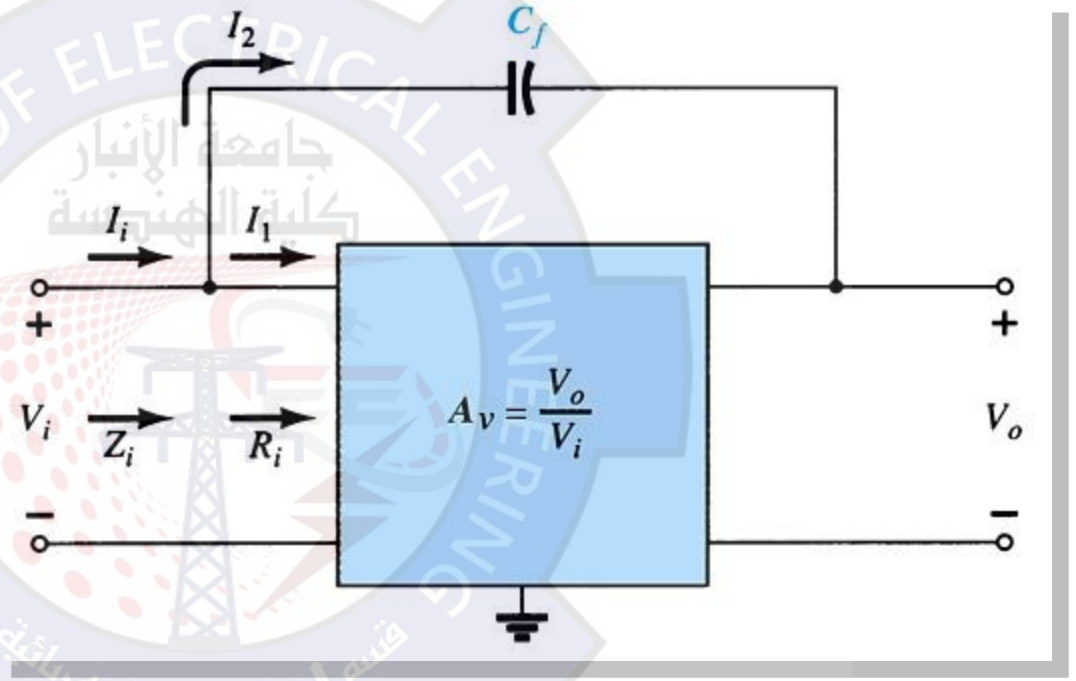
- The base-collector junction at high frequencies in common-emitter BJT amplifier configurations
- The gate-drain junction at high frequencies in common-source FET amplifier configurations.

These capacitances are represented as separate input and output capacitances, called the **Miller Capacitances**.

Miller Input Capacitance (C_{Mi})

$$C_{Mi} = (1 - A_v)C_f$$

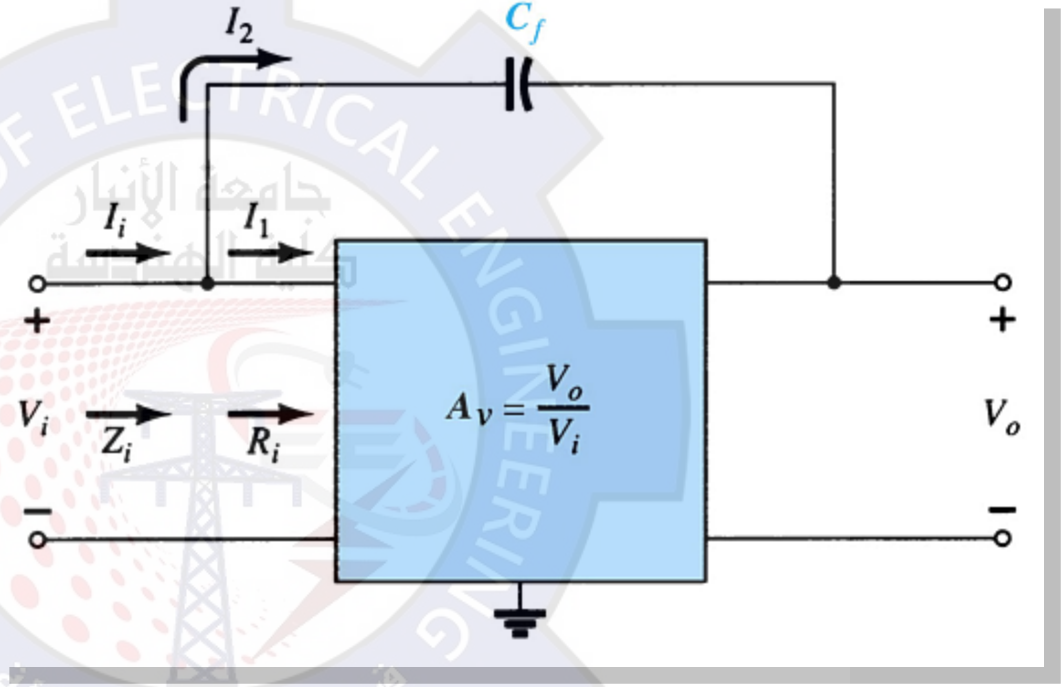
Note that the amount of Miller capacitance is dependent on inter-electrode capacitance from input to output (C_f) and the gain (A_v).



Miller Output Capacitance (C_{Mo})

If the gain (A_v) is considerably greater than 1, then

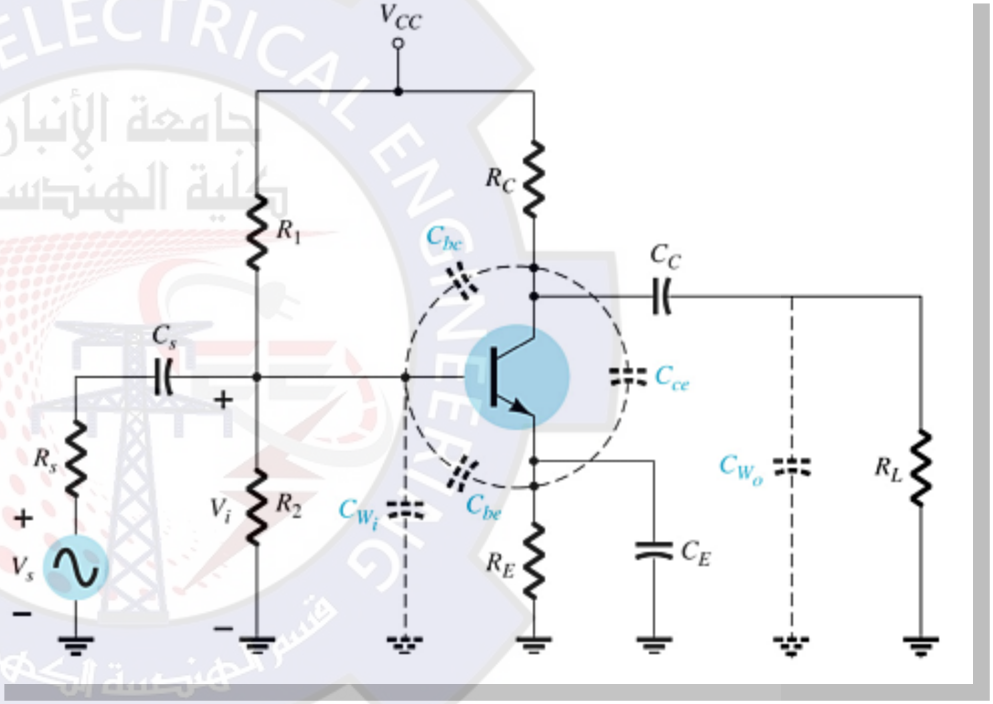
$$C_{Mo} \cong C_f$$



BJT Amplifier High-Frequency Response

Capacitances that affect the high-frequency response are

- **Junction capacitances**
  C_{be}, C_{bc}, C_{ce}
- **Wiring capacitances**
  C_{wi}, C_{wo}
- **Coupling capacitors**
  C_S, C_C
- **Bypass capacitor**
  C_E



Input Network (f_{Hi}) High-Frequency Cutoff

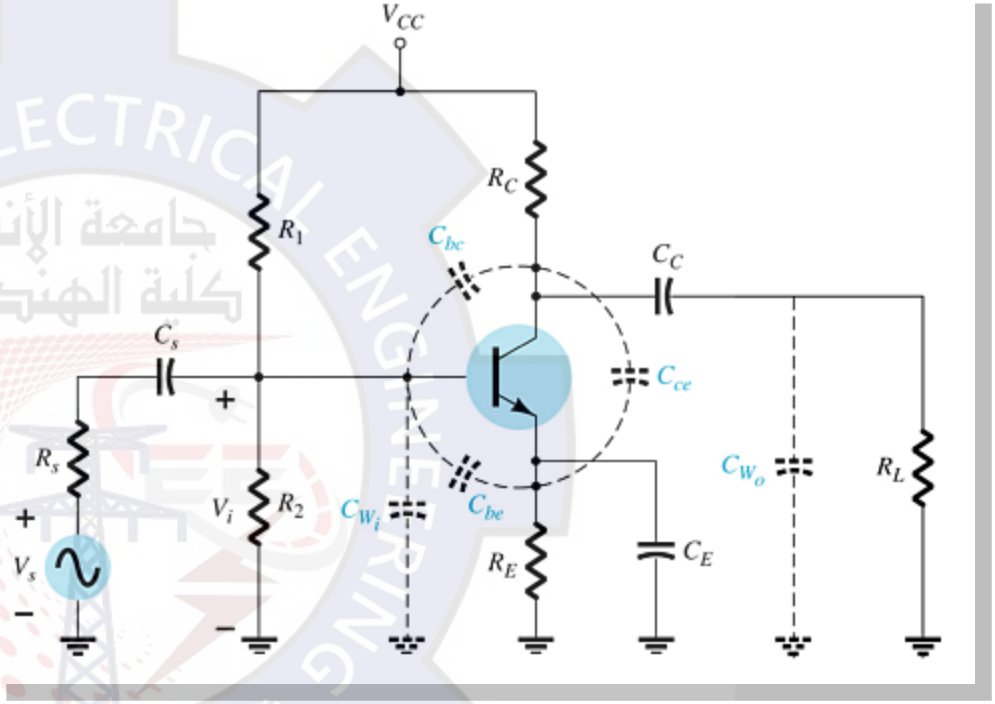
$$f_{Hi} = \frac{1}{2\pi R_{Thi} C_i}$$

where

$$R_{Thi} = R_s \| R_1 \| R_2 \| R_i$$

and

$$C_i = C_{Wi} + C_{be} + C_{Mi}$$
$$= C_{Wi} + C_{be} + (1 - A_v)C_{bc}$$



Output Network (f_{Ho}) High-Frequency Cutoff

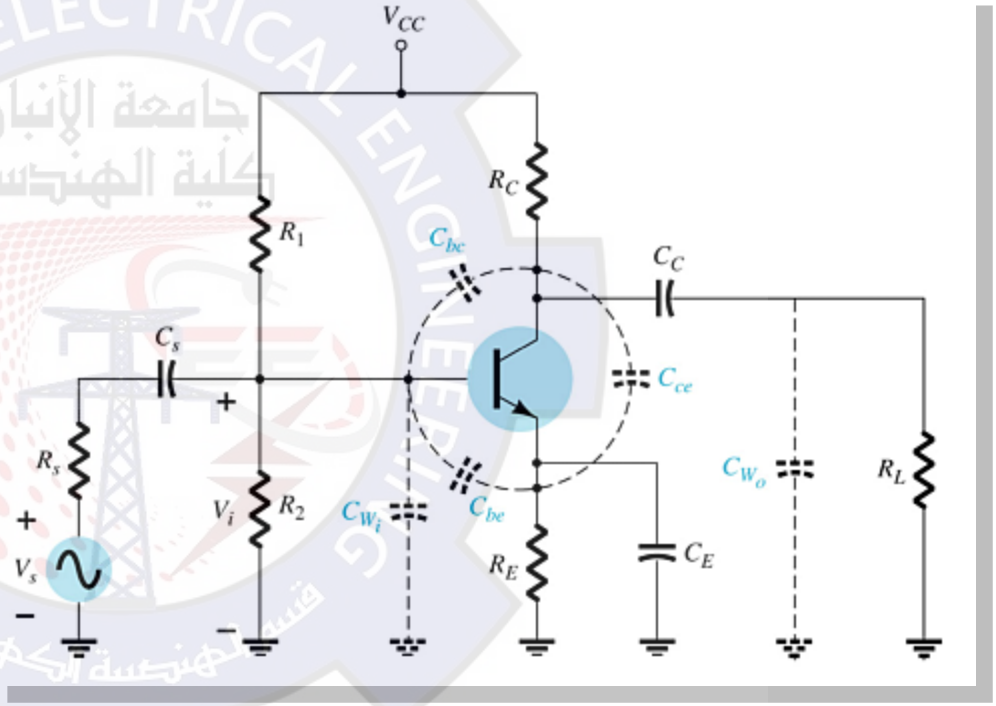
$$f_{Ho} = \frac{1}{2\pi R_{Tho} C_o}$$

where

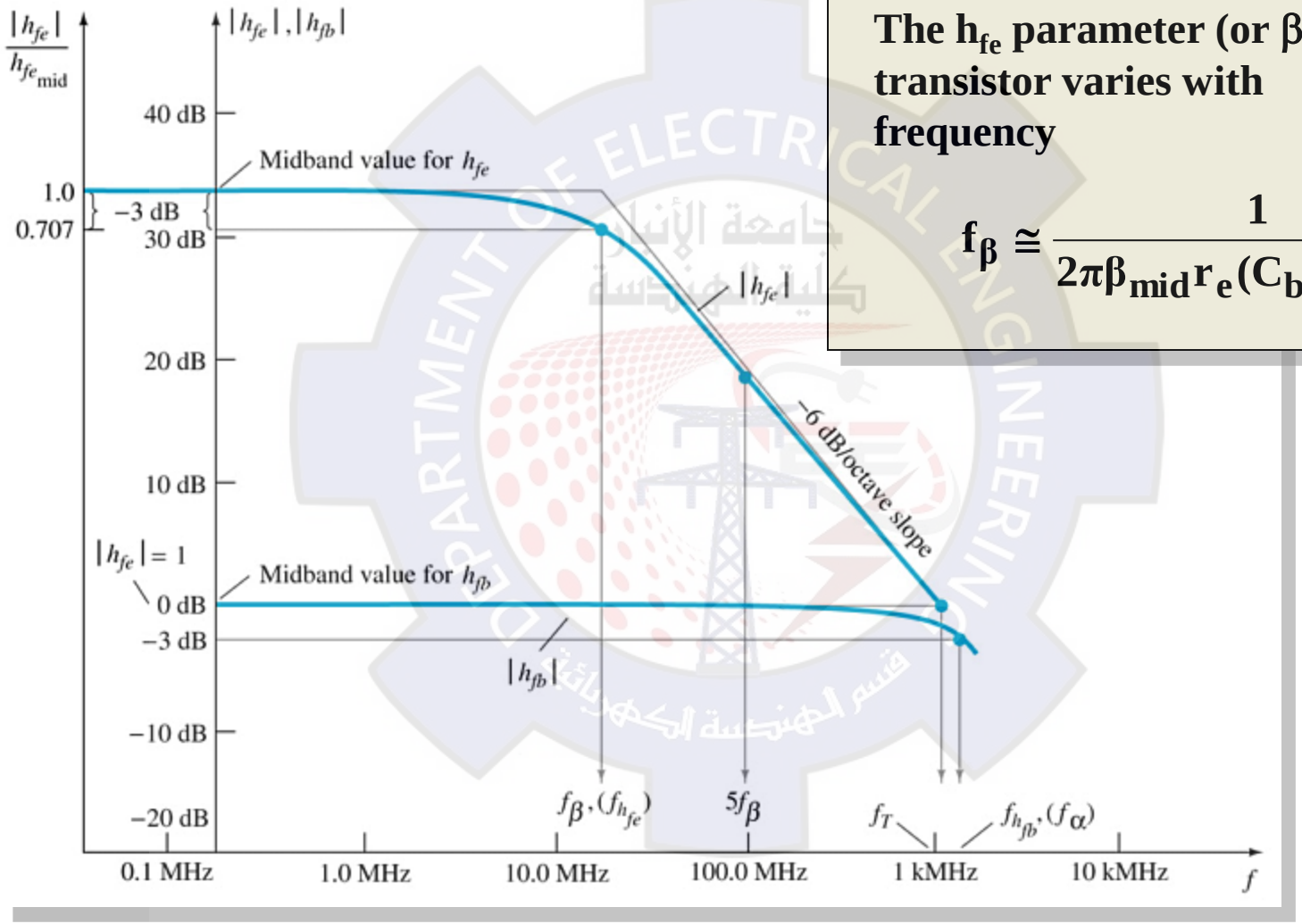
$$R_{Tho} = R_C \| R_L \| r_o$$

and

$$C_o = C_{Wo} + C_{ce} + C_{Mo}$$



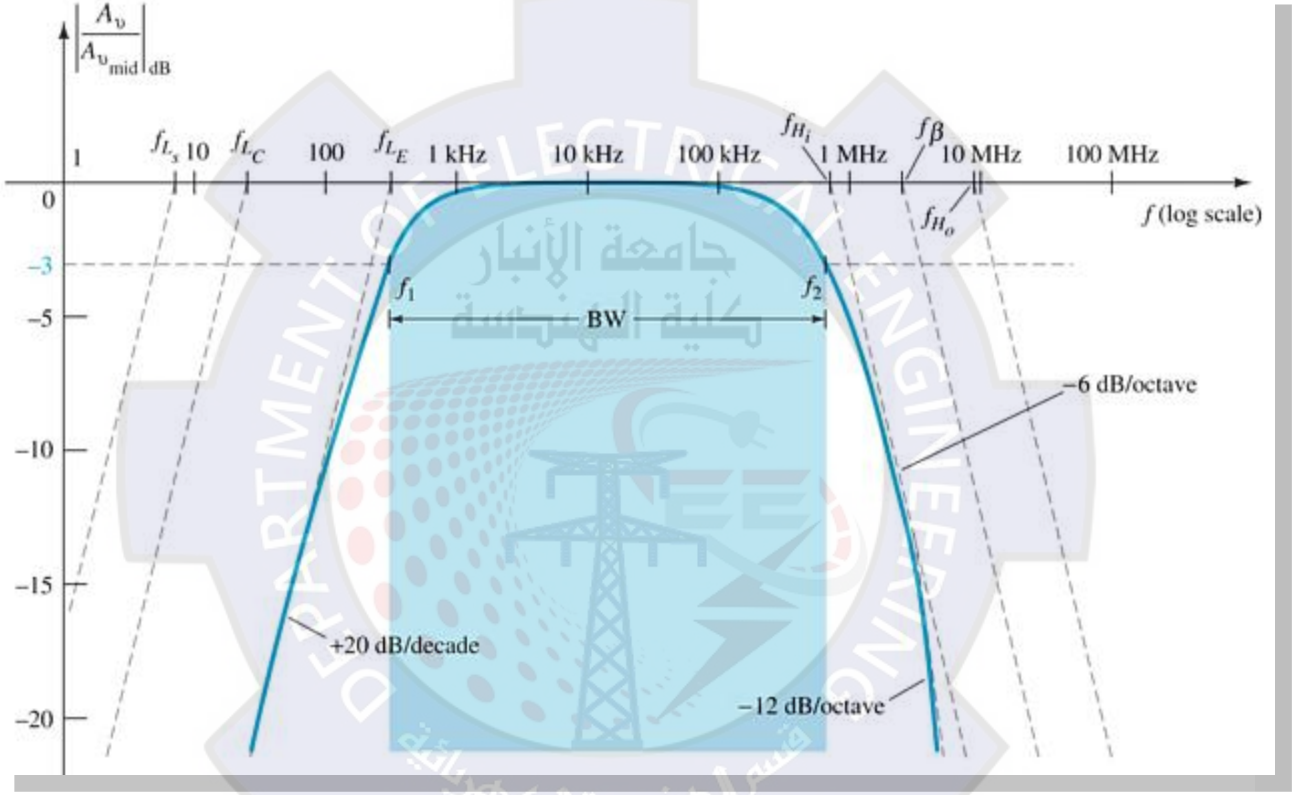
h_{fe} (or β) Variation



The h_{fe} parameter (or β) of a transistor varies with frequency

$$f_\beta \cong \frac{1}{2\pi\beta_{mid} r_e (C_{be} + C_{bc})}$$

BJT Amplifier Frequency Response

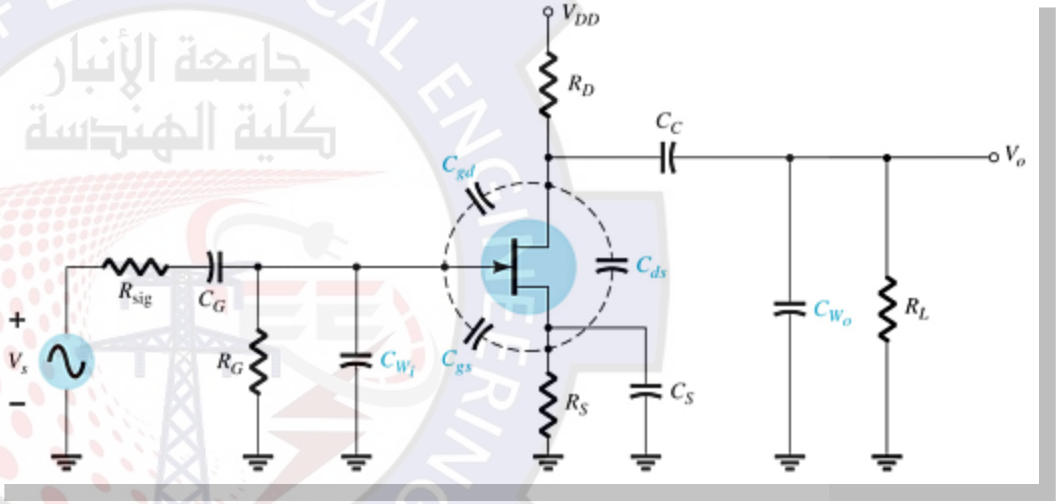


Note the *highest* lower cutoff frequency (f_L) and the *lowest* upper cutoff frequency (f_H) are closest to the actual response of the amplifier.

FET Amplifier High-Frequency Response

Capacitances that affect the high-frequency response are

- **Junction capacitances**
  C_{gs}, C_{gd}, C_{ds}
- **Wiring capacitances**
  C_{wi}, C_{wo}
- **Coupling capacitors**
  C_G, C_C
- **Bypass capacitor**
  C_S



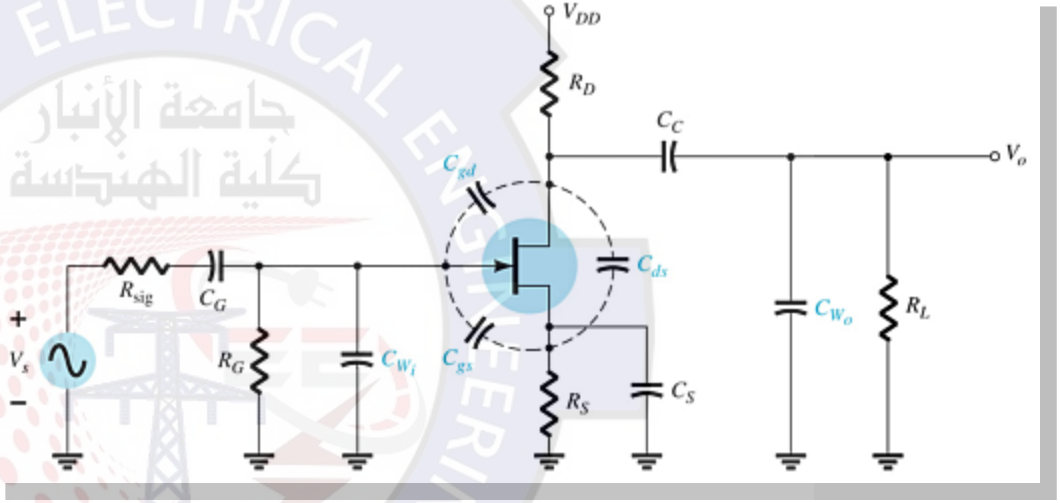
Input Network (f_{Hi}) High-Frequency Cutoff

$$f_{Hi} = \frac{1}{2\pi R_{Thi} C_i}$$

$$C_i = C_{Wi} + C_{gs} + C_{Mi}$$

$$C_{Mi} = (1 - A_v)C_{gd}$$

$$R_{Thi} = R_{sig} \| R_G$$



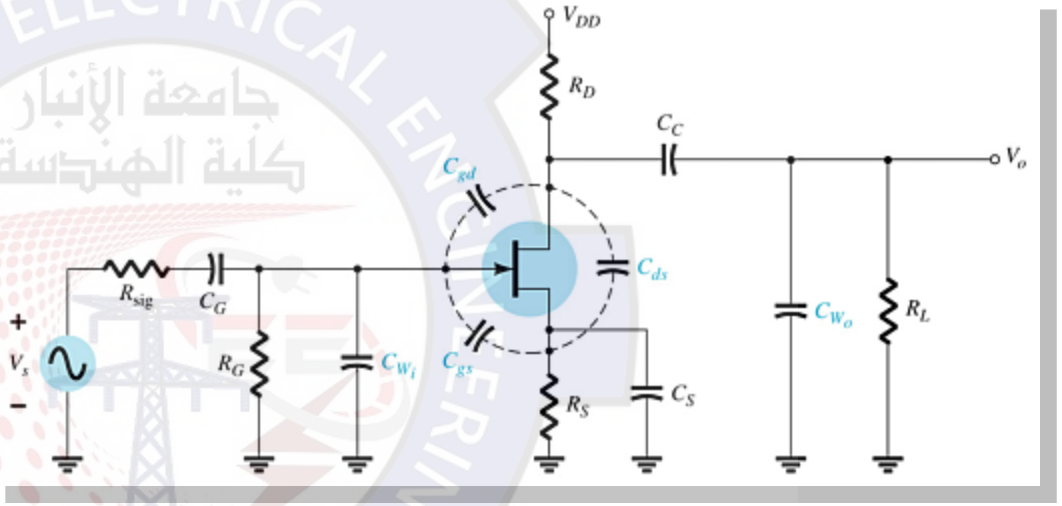
Output Network (f_{Ho}) High-Frequency Cutoff

$$f_{Ho} = \frac{1}{2\pi R_{Tho} C_o}$$

$$C_o = C_{Wo} + C_{ds} + C_{Mo}$$

$$C_{Mo} = \left(1 - \frac{1}{A_v}\right) C_{gd}$$

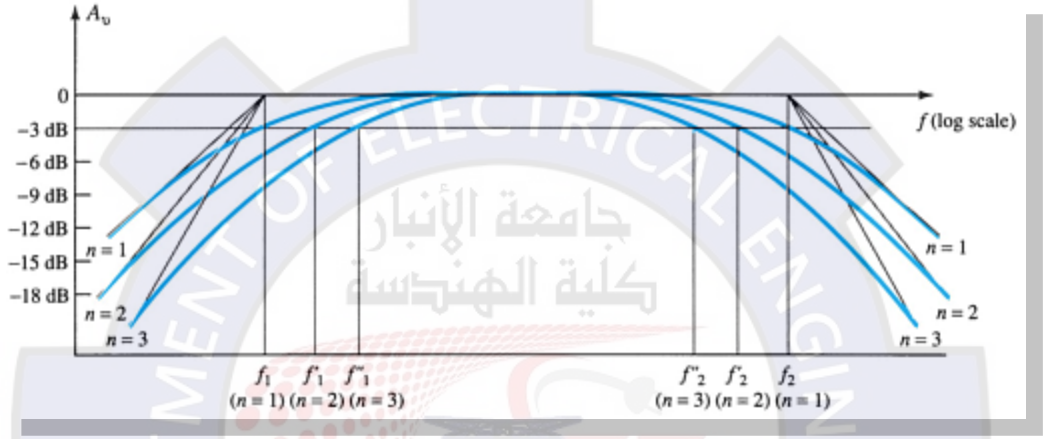
$$R_{Tho} = R_D \,||\, R_L \,||\, r_d$$



Multistage Frequency Effects

Each stage will have its own frequency response, but the output of one stage will be affected by capacitances in the subsequent stage. This is especially so when determining the high frequency response. For example, the output capacitance (C_o) will be affected by the input Miller Capacitance (C_{Mi}) of the next stage.

Multistage Amplifier Frequency Response



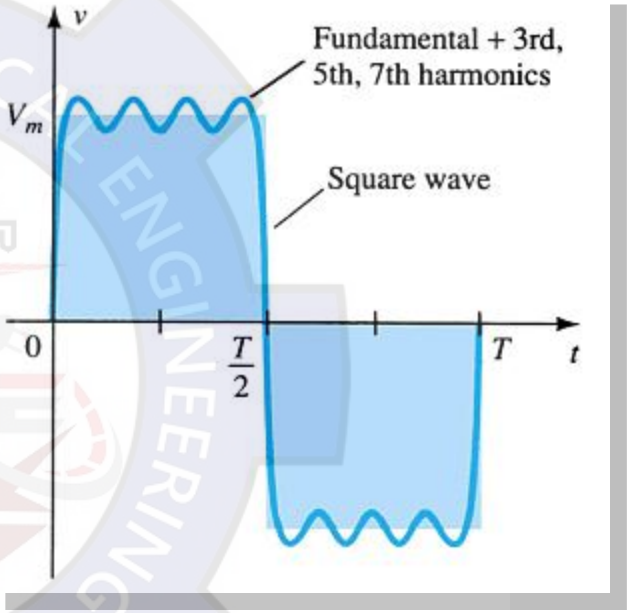
Once the cutoff frequencies have been determined for each stage (taking into account the shared capacitances), they can be plotted.

Note the *highest* lower cutoff frequency (f_L) and the *lowest* upper cutoff frequency (f_H) are closest to the actual response of the amplifier.

Square Wave Testing

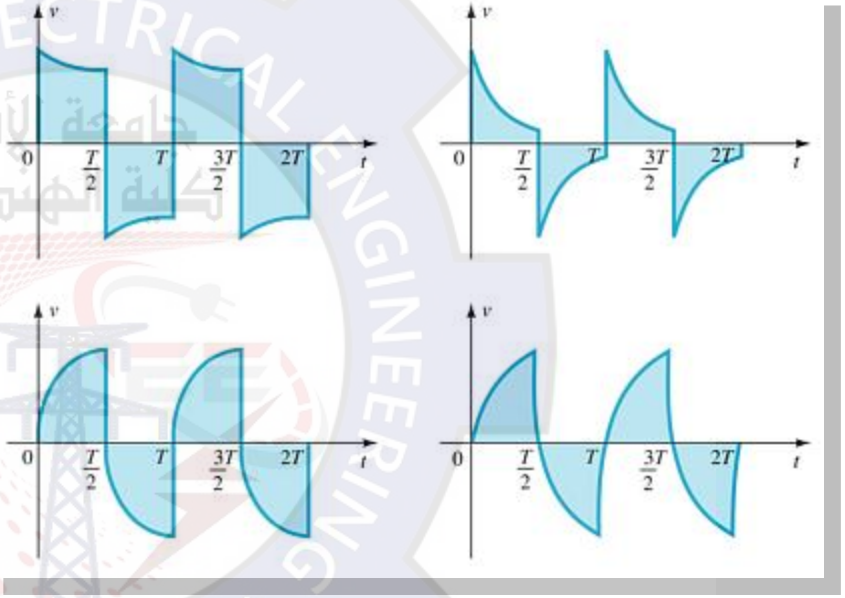
In order to determine the frequency response of an amplifier by experimentation, you must apply a wide range of frequencies to the amplifier.

One way to accomplish this is to apply a square wave. A square wave consists of multiple frequencies (by Fourier analysis: it consists of odd harmonics).



Square Wave Response Waveforms

If the output of the amplifier is not a perfect square wave then the amplifier is 'cutting' off certain frequency components of the square wave.



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Chapter 12

Chapter 12_Compound Configurations

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2018-2019

Chapter 12:
Compound Configurations

Robert Boylestad
Digital Electronics

Cascade Connection

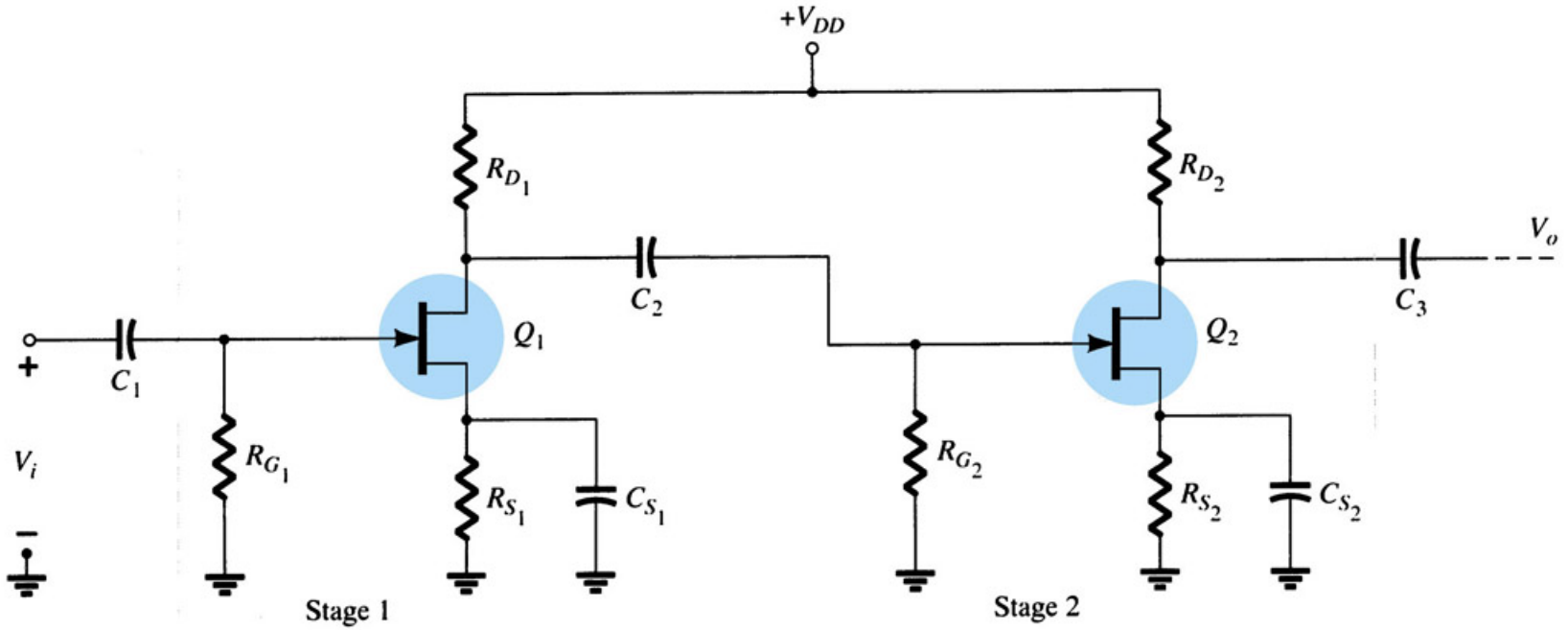
The output of one amplifier is the input to the next amplifier.

The overall gain:

$$\text{Avtotal: } Av_1 * Av_2$$

Note the DC bias circuits are isolated from each other by the coupling capacitors.
The DC calculations are independent of the cascading.
The AC calculations for gain and impedance are interdependent.

FET Cascade Amplifier

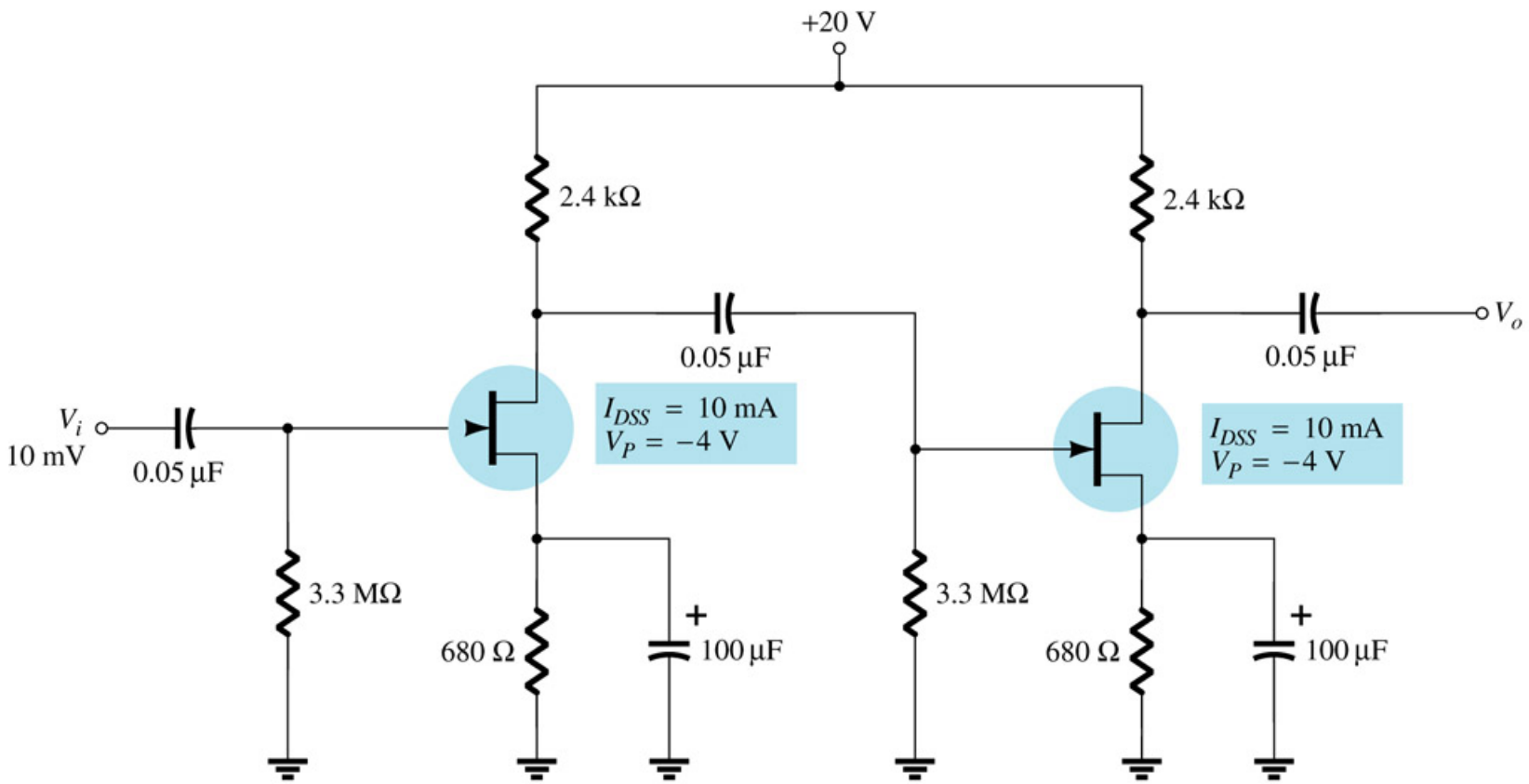


Voltage Gain: $Av = Av_1Av_2 = (-g_{m1}R_{D1})(-g_{m2}R_{D2})$ [Formula 12.1]

Input Impedance: $Zi = R_{G1}$ [Formula 12.2]

Output Impedance: $Zo = R_{D2}$ [Formula 12.3]

Example of a Cascaded FET Amplifier



DC Calculations

From the DC Bias Calculations:

VGSQ = -1.9V

IDQ = 2.8mA

Both transistors: $$gm_0 = \frac{2I_{DSS}}{|Vp|} = \frac{2(10mA)}{|-4V|} = 5mS$$

At the bias point: $$gm = gm0\left(1 - \frac{V_{GSQ}}{Vp}\right) = (5mS)\left(1 - \frac{-1.9v}{-4v}\right) = -2.6mS$$

AC Gain and Output Voltage

Voltage gain of each stage:

$$Av_1 = Av_2 = -gmR_D = -(2.6mS)(2.4k\Omega) = -6.3$$

The cascaded amplifier gain:

$$Av = Av_1 * Av_2 = (-6.2)(-6.2) = 38.4$$

The output voltage:

$$Vo = Av * Vi = (38.4)(10mV) = 383mV$$

Impedances and Loaded Output Voltage

Input Impedance:

$$Zi = RG = 3.3M\Omega$$

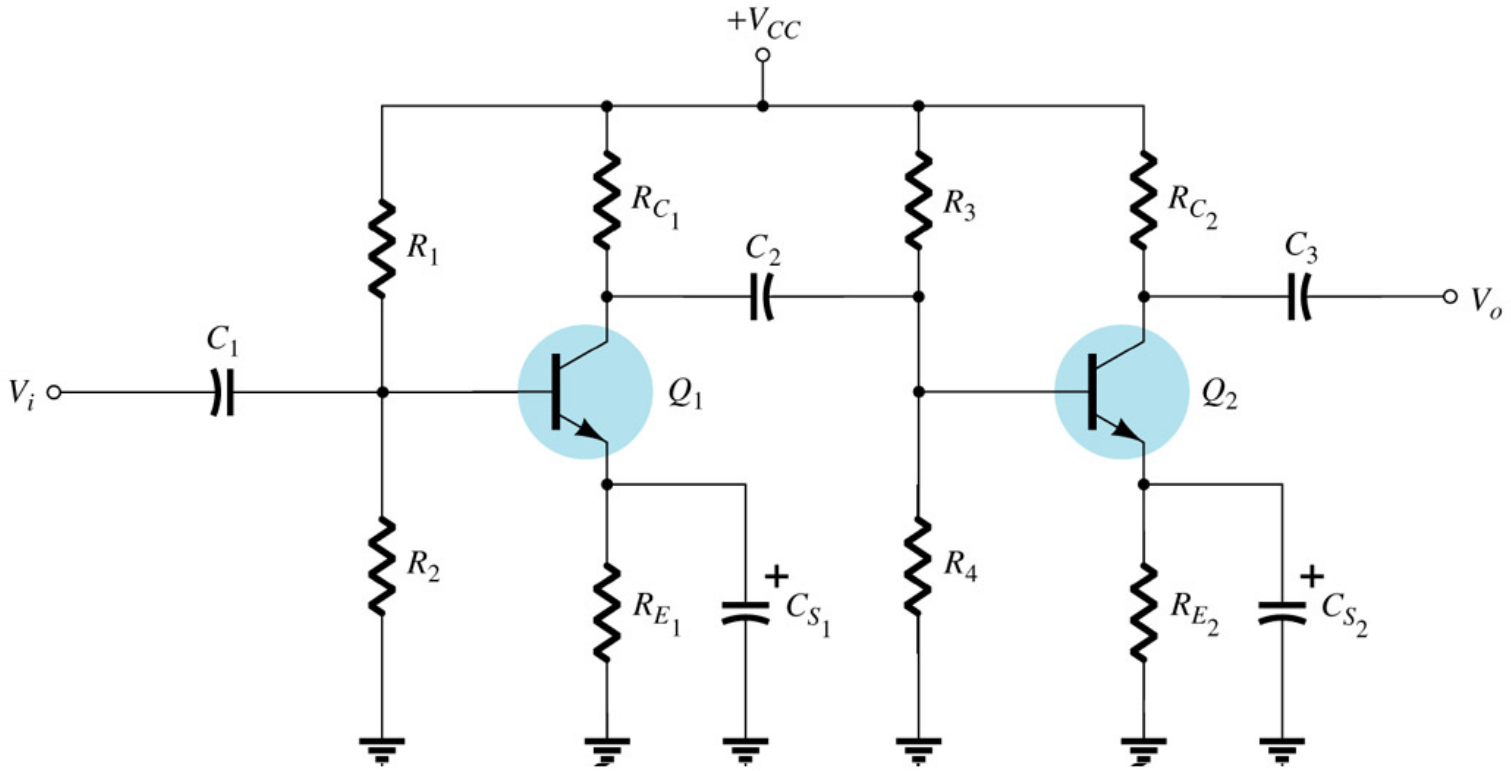
Output Impedance:

$$Zo = RD = 2.4k\Omega$$

Output across a 10kΩ load:

$$VL = \frac{R_L}{Zo + R_L} Vo = \frac{10k\Omega}{2.4k\Omega + 10k\Omega} 384mV = 310mV$$

BJT Cascade Amplifier



Voltage Gain: $$Av = \frac{-R_C \parallel R_L}{r_e}$$ [Formula 12.4]

Input Impedance: $$Zi = R_1 \parallel R_2 \parallel \beta r_e$$ [Formula 12.5]

Output Impedance: $$Zo = R_C \parallel r_o$$ [Formula 12.6]

DC Calculations

From the DC Bias Calculations:

VB = 4.7V

VE = 4.0V

VC = 11V

IE = 4.0mA

re = 6.5Ω

AC Gain and Output Voltage

Voltage gain of each stage:

$$Av1 = -\frac{(R_C \,||\, R_1 \,||\, R_2 \,||\, \beta r_e)}{r_e}$$

$$Av1 = -\frac{(2.2k\Omega \,||\, 15k\Omega \,||\, 4.7k\Omega \,||\, (200)(6.5\Omega)}{6.5\Omega} = -102.3$$

$$Av2 = -\frac{R_C}{r_e} = -\frac{2.2k\Omega}{6.5\Omega} = -338.46$$

The cascaded amplifier gain:

$$Av = Av1 * Av2 = (-102.3)(-338.46) = 34{,}624$$

The output voltage:

$$Vo = Av * Vi = (34{,}624)(.025mV) = 0.866V$$

Impedances and Loaded Output Voltage

Input Impedance:

$$Zi = R_1 \parallel R_2 \parallel \beta r_e = 15k\Omega \parallel 4.7k\Omega \parallel (200)(6.5\Omega) = 953.6\Omega$$

Output Impedance:

$$Zo = RC = 2.2k\Omega$$

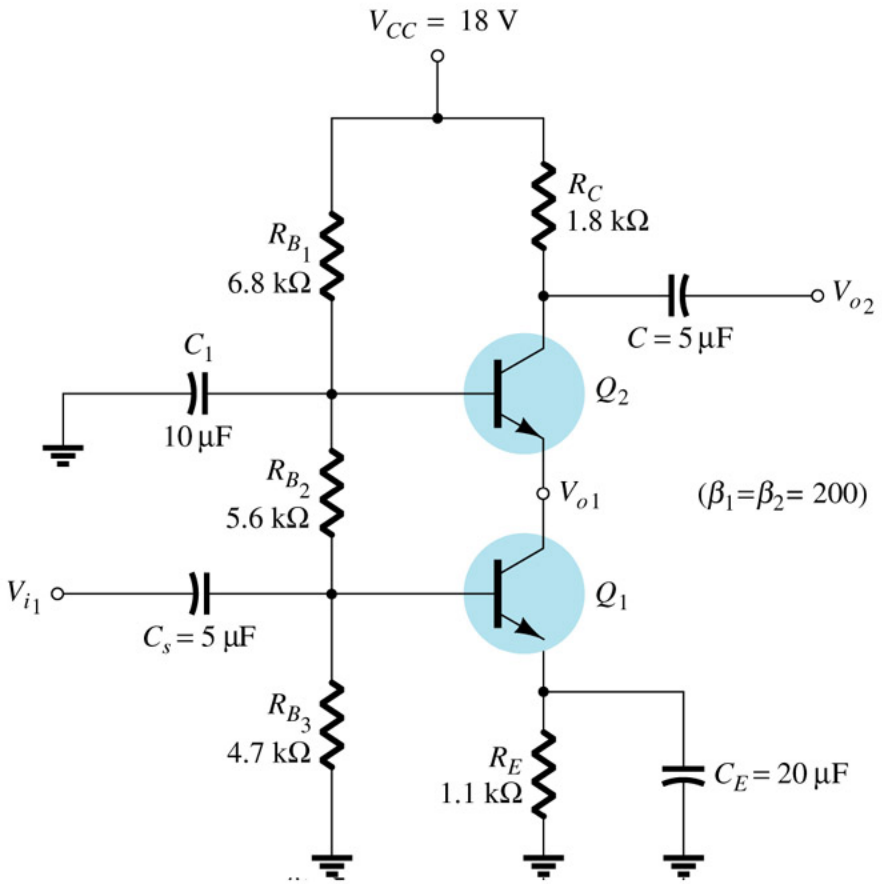
Output across a 10kΩ load:

$$VL = (R_L / (Zo + R_L)) * Vo = (10k\Omega /(2.2k\Omega + 10k\Omega)) * .866V = .71V$$

Combination of FET and BJT Cascade

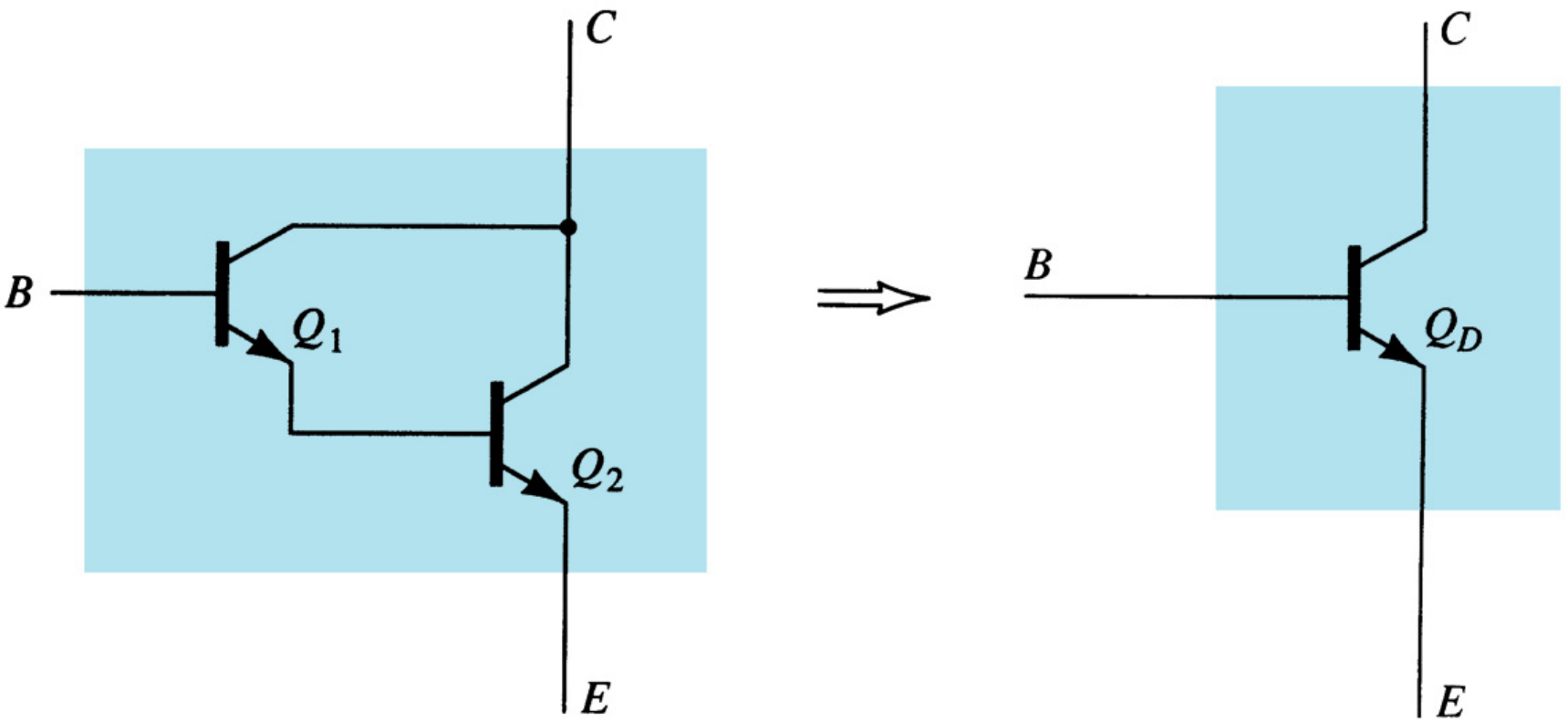
A FET-BJT cascade is calculated in a similar fashion as a FET-FET or a BJT-BJT cascade. This combination provides a high gain from the BJT with the high input impedance from the FET.

Cascode Connection



This is a CE – CB combination.
This arrangement provides high input impedance but a low voltage gain.
The low voltage gain reduces the Miller Input Capacitance therefore this combination works well in high frequency applications.

Darlington Connection



This combination provides large current gain, typically a few thousand.

It has a voltage gain of near 1, a low output impedance and a high input impedance.

Packaged Darlington Transistor

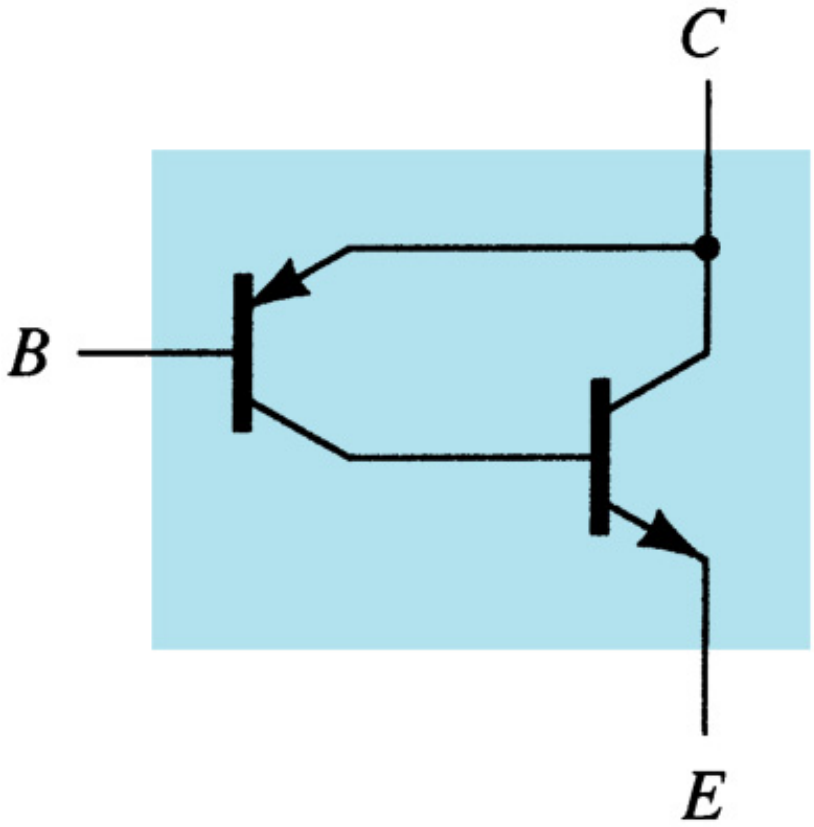
Type 2N999

N-P-N Darlington-Connected Silicon Transistor Package

Parameter	Test Conditions	Min.	Max.
V_{BE}	$I_C = 100$ mA		1.8 V
h_{FE} (β_D)	$I_C = 10$ mA	4000	
	$I_C = 100$ mA	7000	70,000

Darlington transistor is available in a single package.

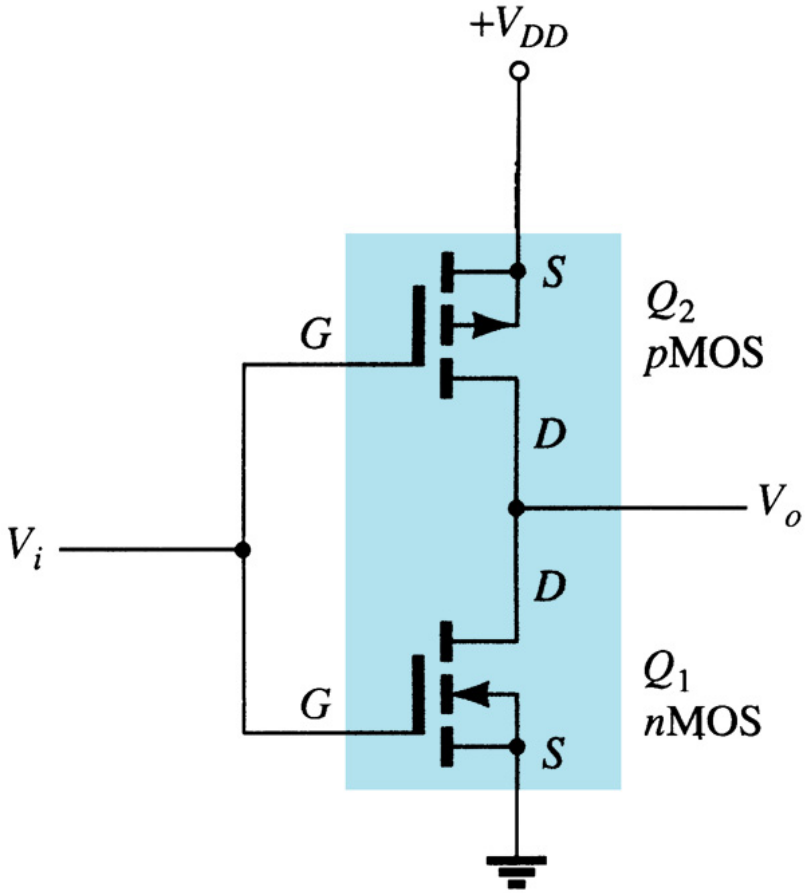
Feedback Pair



This is a two-transistor circuit that operates like a Darlington pair.
It has similar characteristics: high current gain, voltage gain of near 1, low output impedance and high input impedance.
Note: it is ***not the Darlington*** configuration:

Darlington: 2 npn BJTs
Feedback Pair: pnp driving an npn BJT

CMOS Circuit



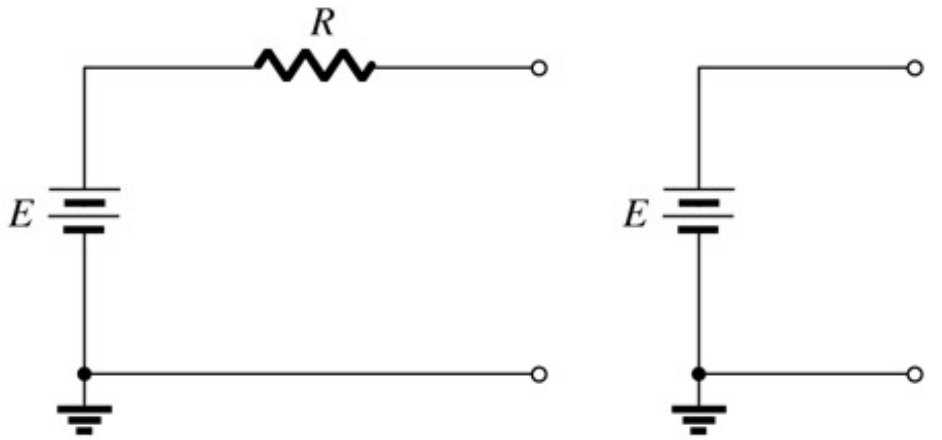
This CMOS circuit is used in integrated digital circuitry.
It uses both n-channel and p-channel enhancement MOSFET transistors. This arrangement is called a Complementary MOSFET (or CMOS).

The input is applied to both gates and the output is from the connected drains.

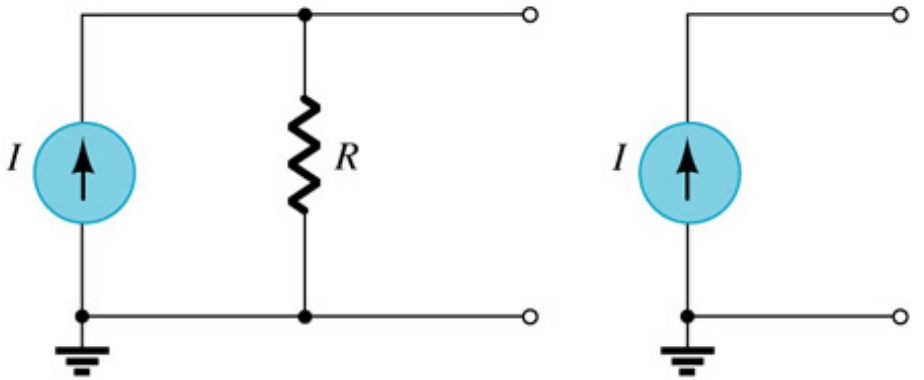
Voltage vs. Current Source

Voltage Source

The ideal voltage source provides a constant voltage to any load and it has an internal resistance of zero.



(a)



(b)

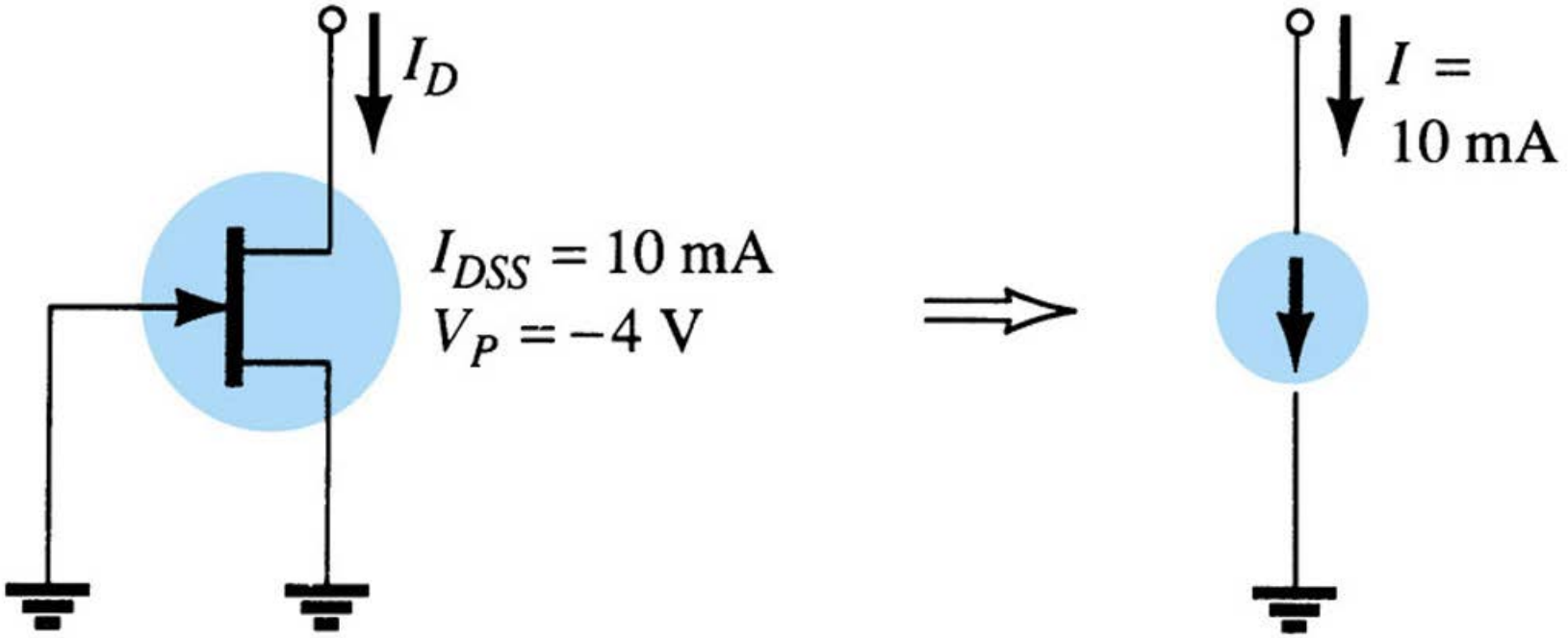
Current Source

The ideal current source provides a constant current to any load and has an infinite internal resistance.

Current Source Circuits

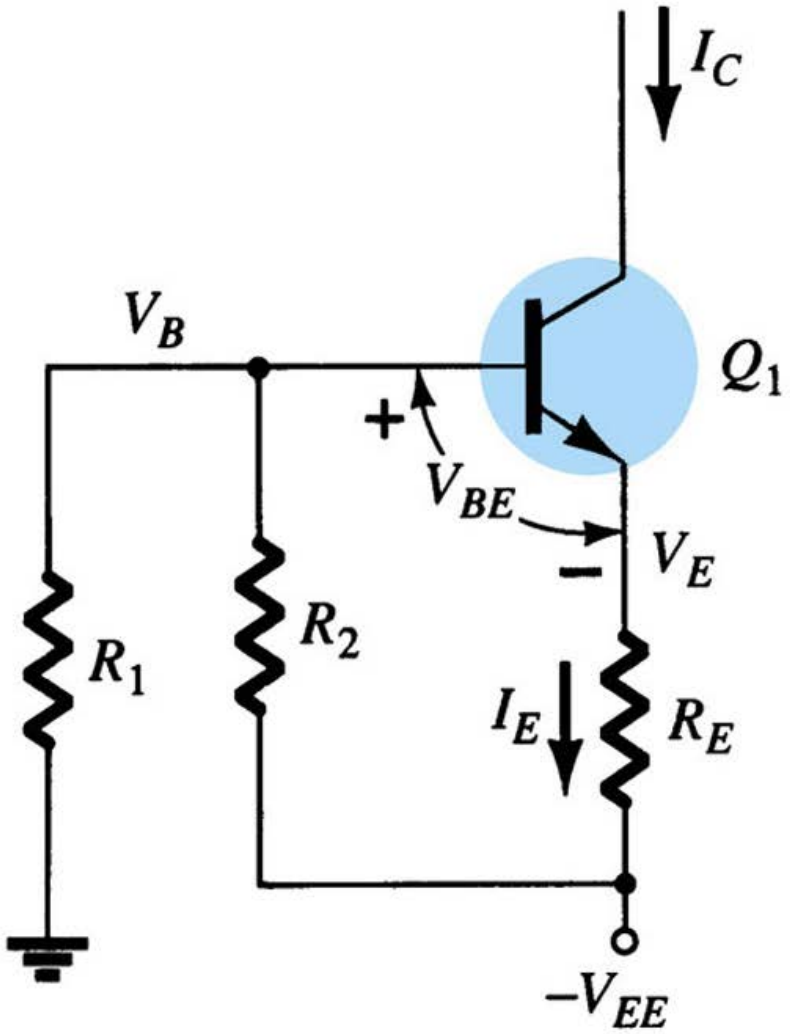
Constant-current sources can be built using FETs, BJTs and a combination of these devices.

JFET Current Source



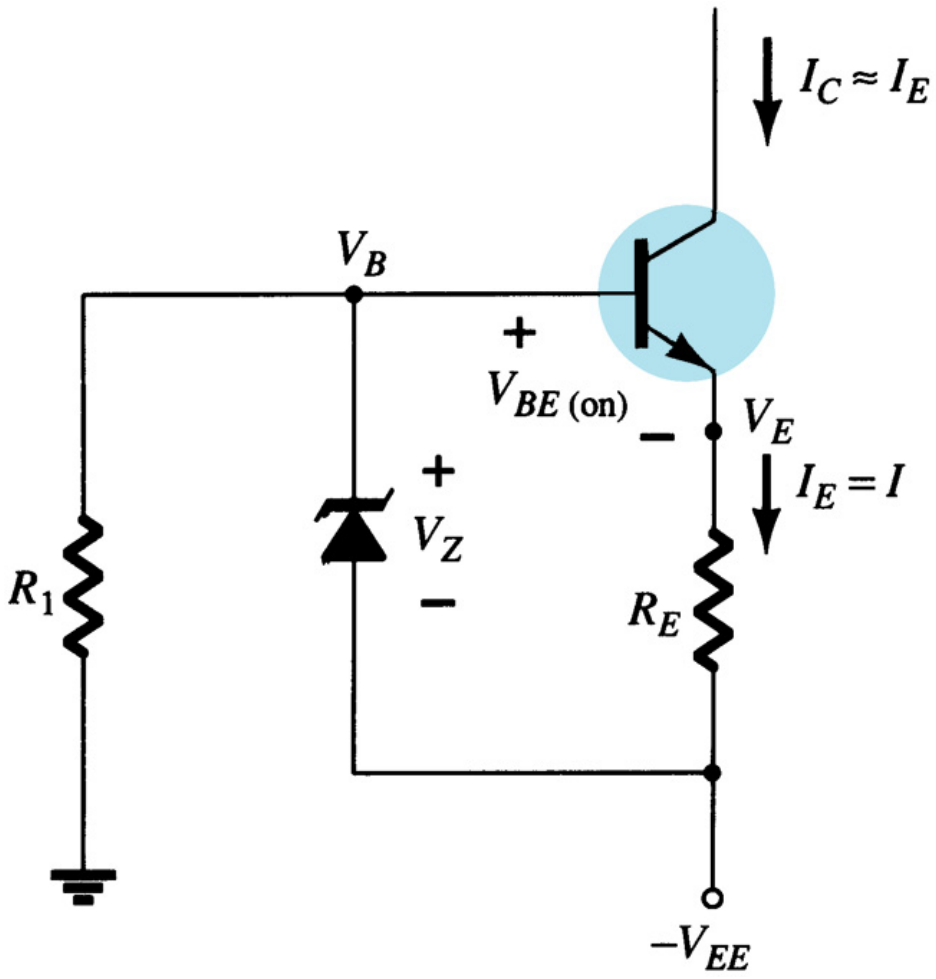
$V_{GS} = 0V$ and $I_D = I_{DSS} = 10mA$

BJT Constant Current Source



$$I_E \cong I_C$$

Transistor/Zener Constant Current Source

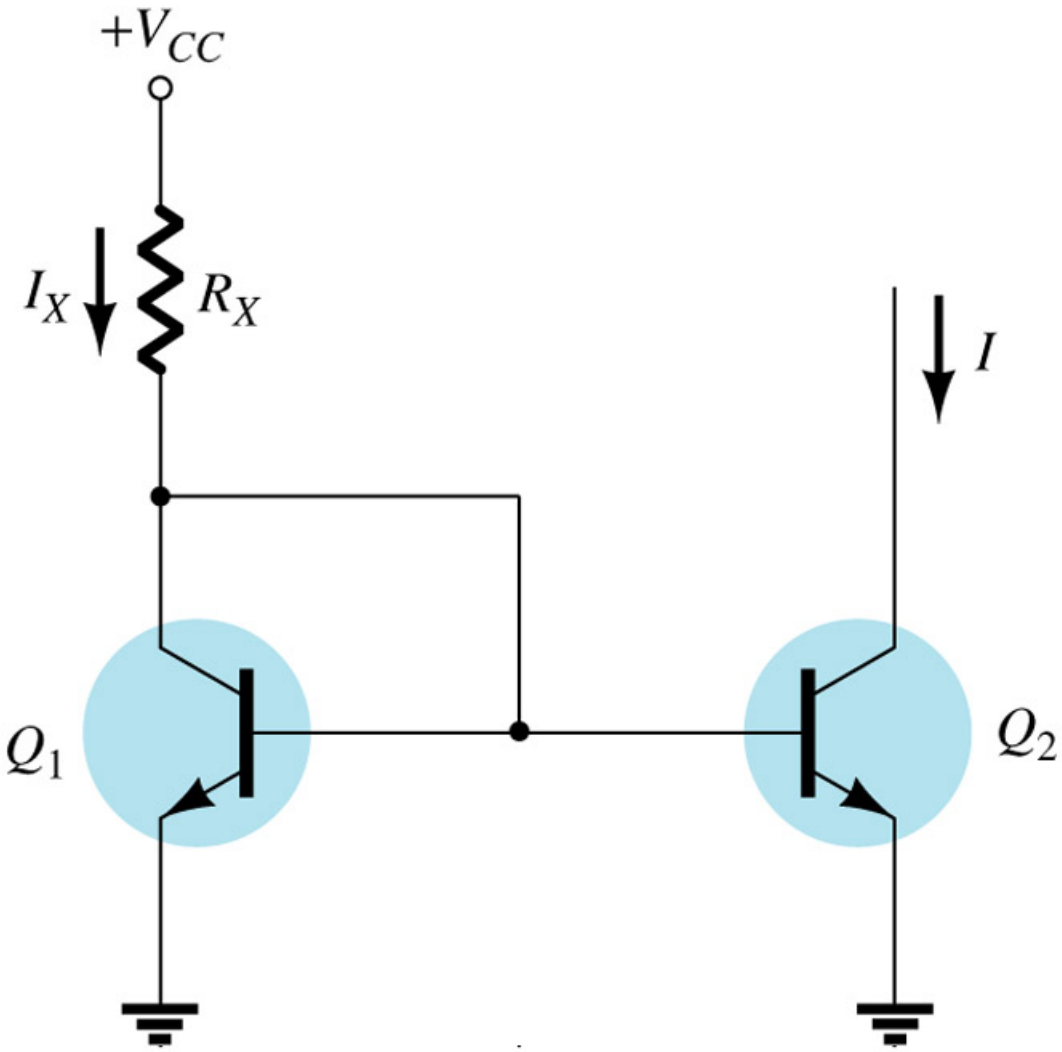


Replacing resistor R2 with a Zener improves the constant current source.

$$I \approx I_E = \frac{V_Z - V_{BE}}{R_E}$$

[Formula 12.26]

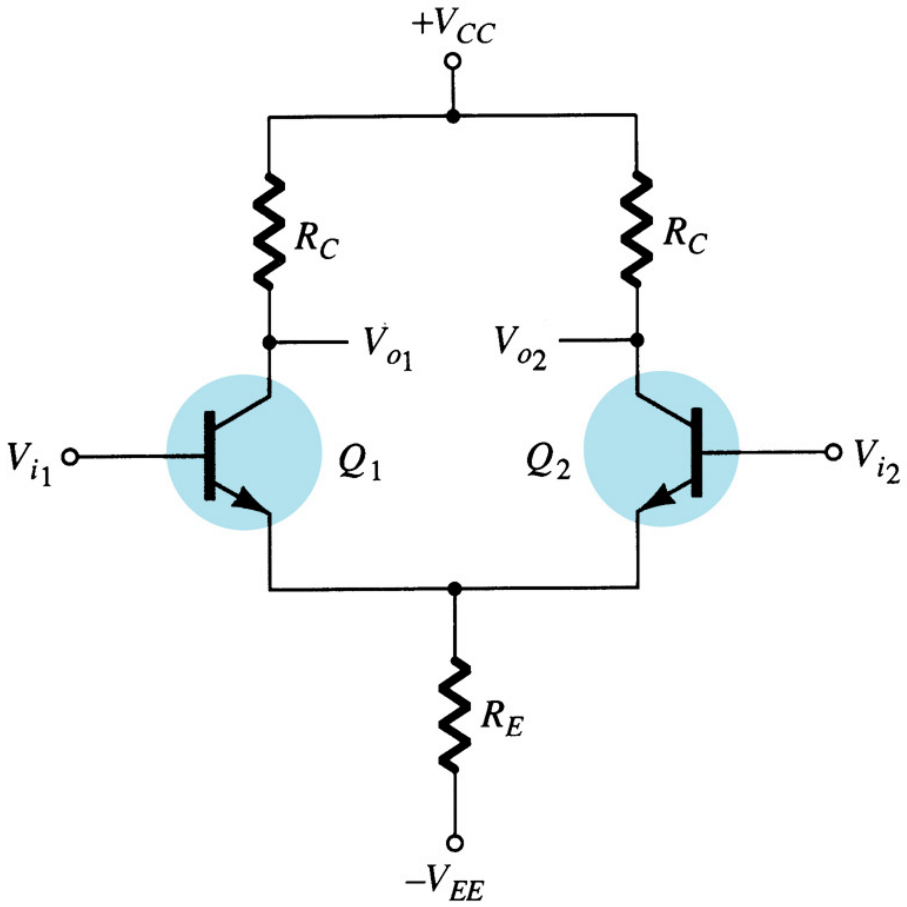
Current Mirror Sources

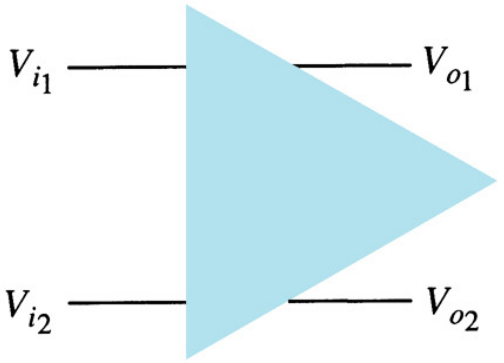


Current Mirror circuits are used to provide constant current in integrated circuits.

Differential Amplifier Circuit

Differential amplifier circuits have 2 inputs and 2 outputs.





It can be operated with a dual power supply: V_{CC} to V_{EE};
or with a single supply: V_{CC} to G_{ND}

Features of Differential Amplifiers

- It amplifies the difference between the 2 inputs
- It is a high gain, low noise amplifier

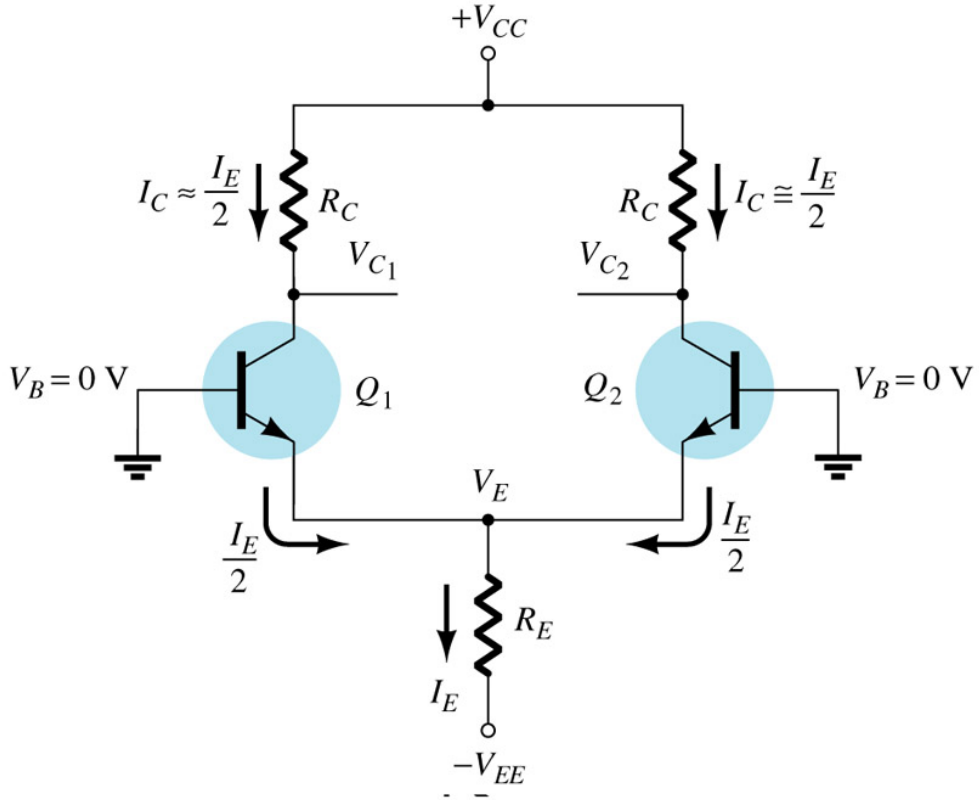
3 Modes of Operation

1. Single-ended **~** an input signal is applied to one of the inputs and the other input is grounded.

2. Double-ended **~** two different input signals are applied to the inputs.

3. Common-mode **~** the same input signal is applied to both inputs.

DC Bias



$$V_E = 0V - V_{BE} = -0.7V$$

Both inputs are grounded:

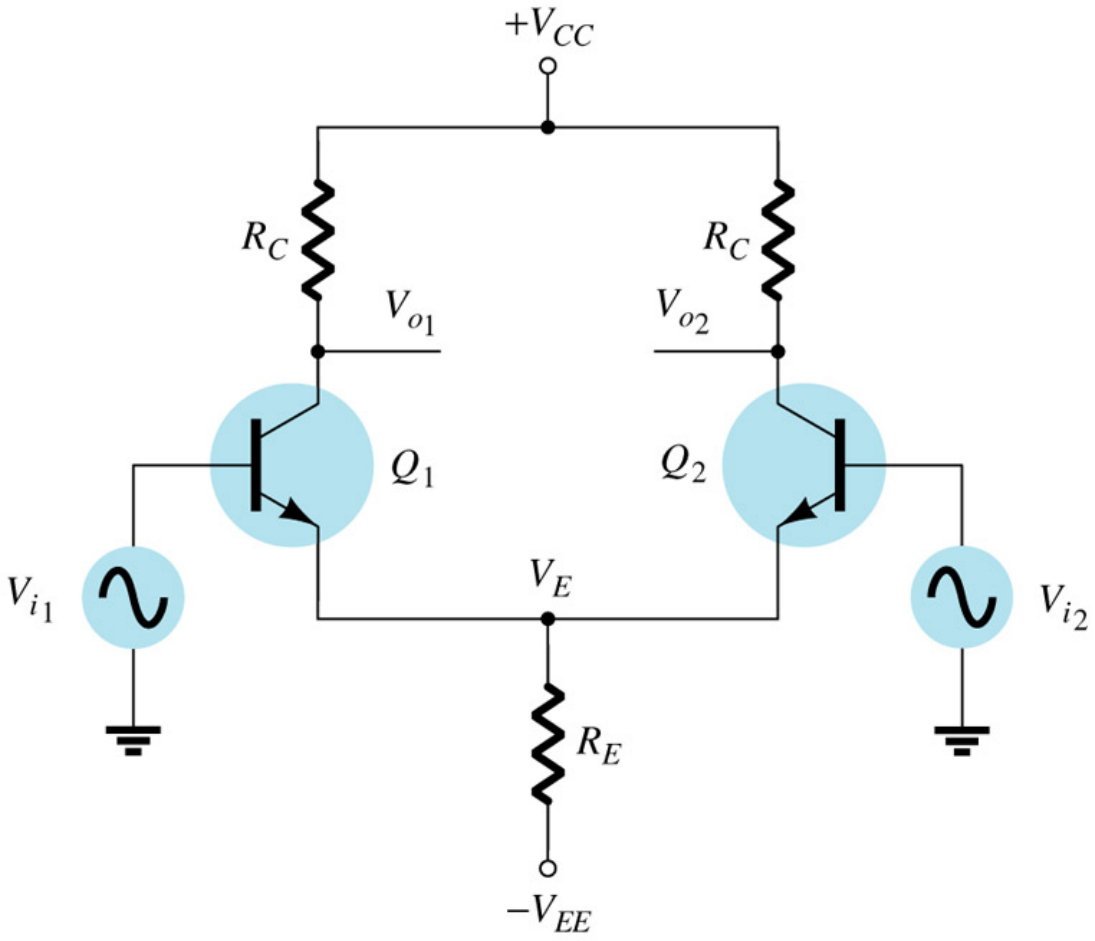
$$I_E = \frac{V_E - (-V_{EE})}{R_E} \approx \frac{V_{EE} - 0.7}{R_E}$$ [Formula 12.28]

assuming both transistors are well matched:

$$I_{C1} = I_{C2} = \frac{I_E}{2}$$ [Formula 12.29]

$$V_{C1} = V_{C2} = V_{CC} - I_C R_C = V_{CC} - \frac{I_E}{2} R_C$$ [Formula 12.30]

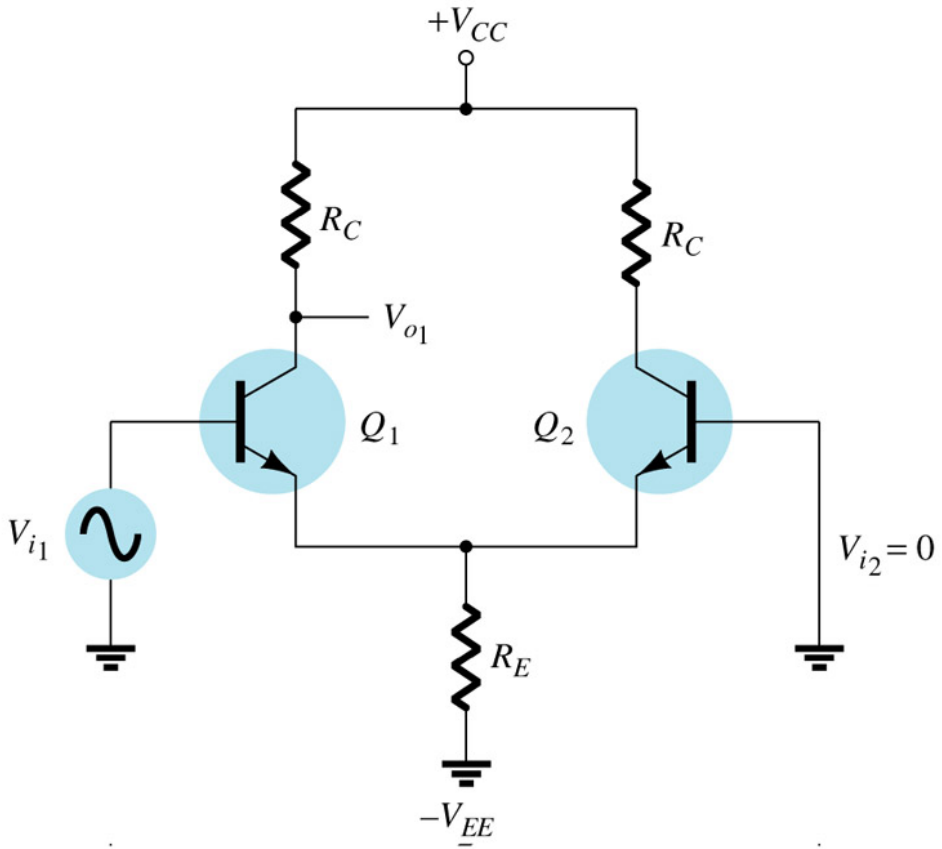
AC Operation



Separate signals are applied to the inputs: Vi_1 and Vi_2
Separate signals are available at the outputs: Vo_1 and Vo_2

Single-Ended Mode AC Voltage Gain

In this mode a signal is connected to one input and the other is grounded.



Assuming the transistor circuits are perfectly matched:

$$Av = \frac{Vo}{Vi_1} = \frac{R_C}{2r_e}$$

[Formula 12.31]

Double-Ended AC Voltage Gain

Double-ended mode connects a different signal to each input.

$$A_d = \frac{V_o}{V_d} = \frac{\beta R_C}{2r_i}$$

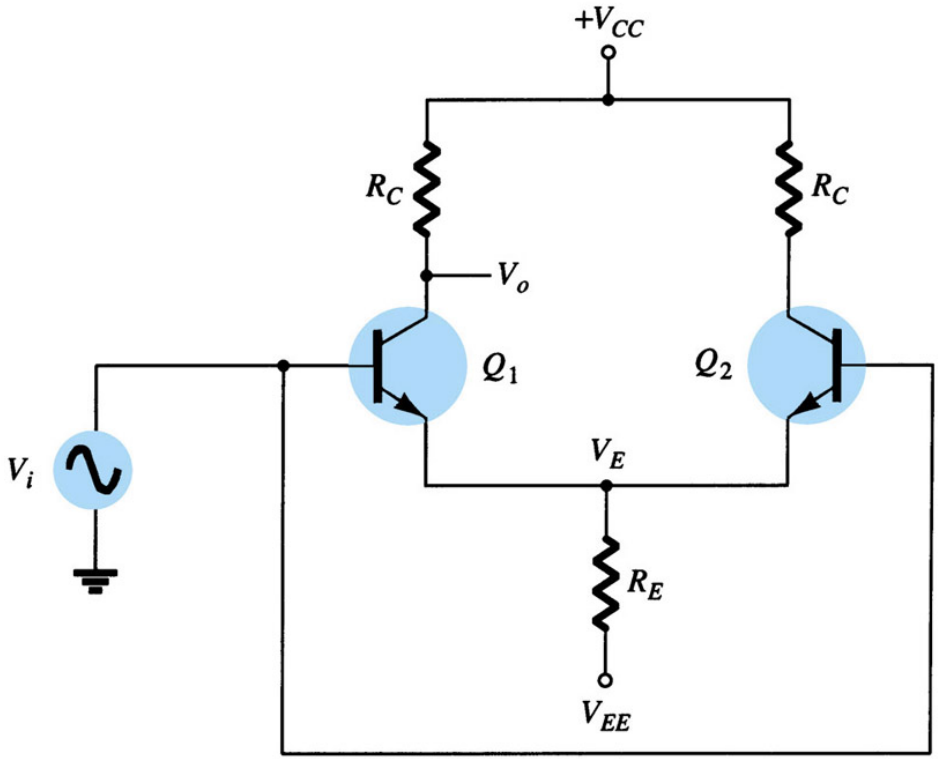
[Formula 12.32]

Where A_d = differential voltage gain

$V_d = V_{i_1} - V_{i_2}$ (the difference between the inputs)

Common-Mode AC Gain

Common-mode applies the same signal to both inputs. Because the amplifier amplifies the difference between the inputs. The common-mode gain should be quite small.



$$Ac = \frac{Vo}{Vi} = \frac{\beta R_C}{r_i + 2(\beta + 1)R_E}$$

[Formula 12.33]

Where Ac = common mode gain

Common-Mode Rejection = Noise Rejection

In common-mode, the signal common to both inputs will have a low gain (Ac).

In differential-mode (single- or double-ended), any signal that is common to both inputs will have a low gain. Any signal, in differential-mode that is common to both inputs is noise.

The ability of the amplifier to have a low common-mode gain, i.e. not amplify signals that are common to both inputs, is called Common-Mode Rejection.

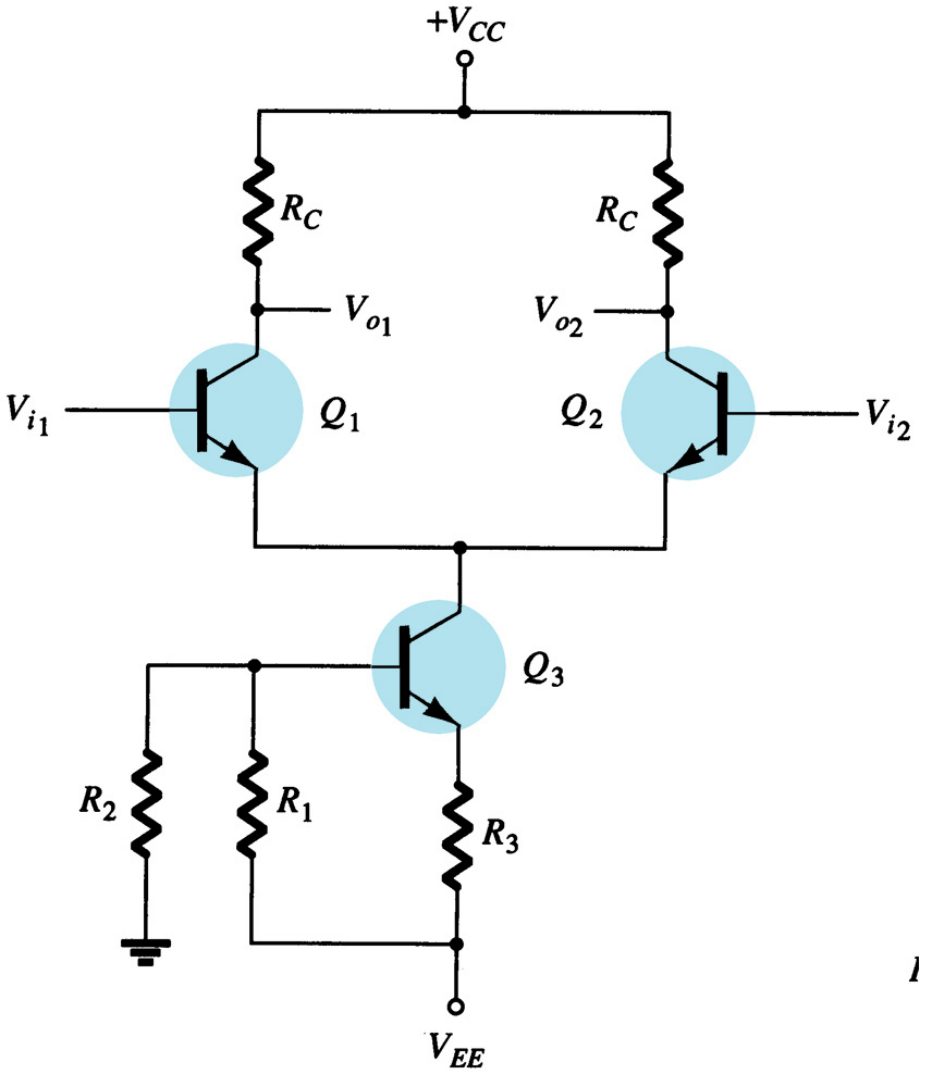
Improving Common-Mode Rejection

To improve common-mode rejection:

- Ad must increase
- Ac must decrease

One method is to increase the value of R_E in AC by adding a constant-current source circuit.

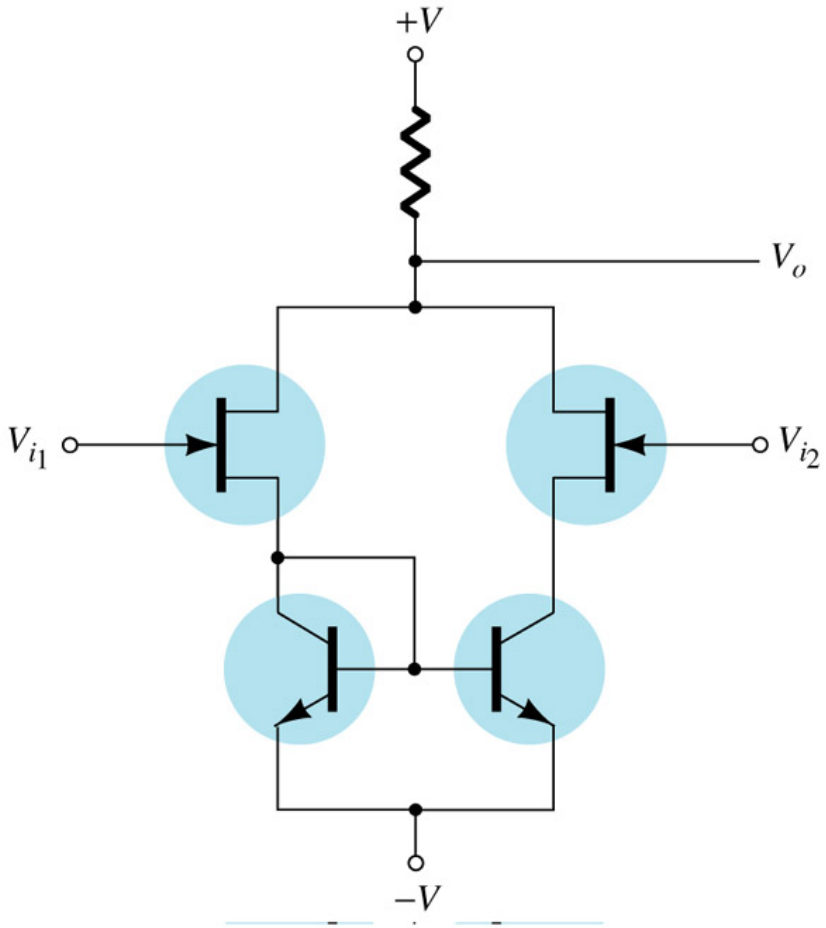
Constant-Current Source Circuit



This increases the AC impedance for R_E.

BIFET Differential Amplifier Circuit

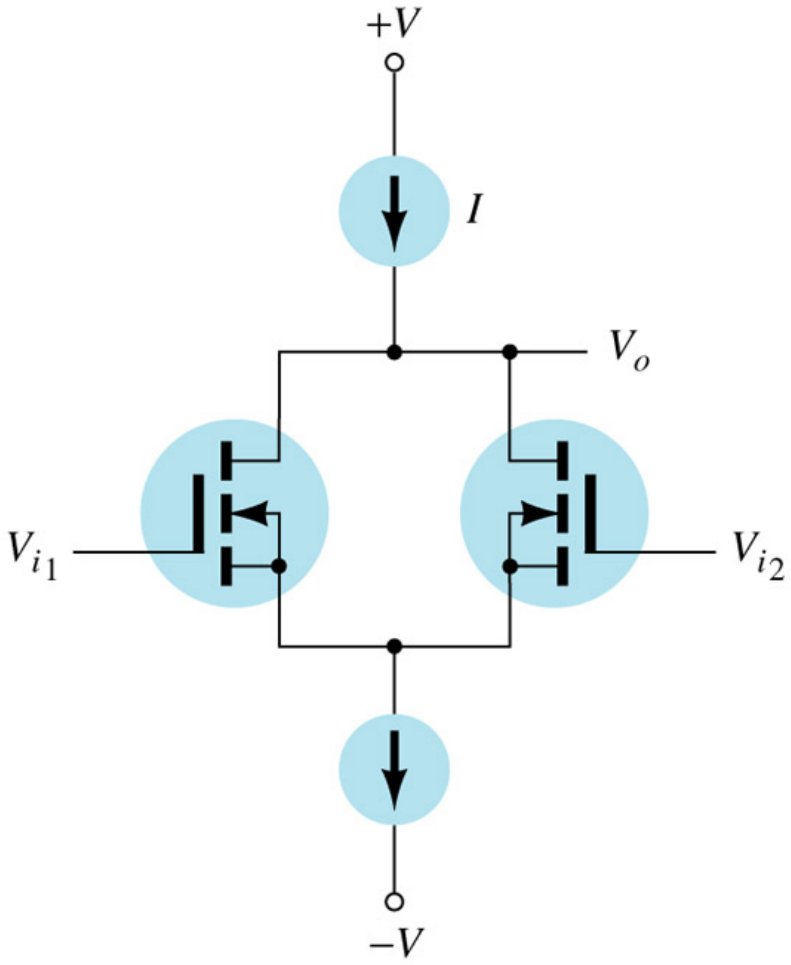
The differential amplifier characteristics can be improved by using JFETs as input transi



BIFET circuit increases the input impedance.

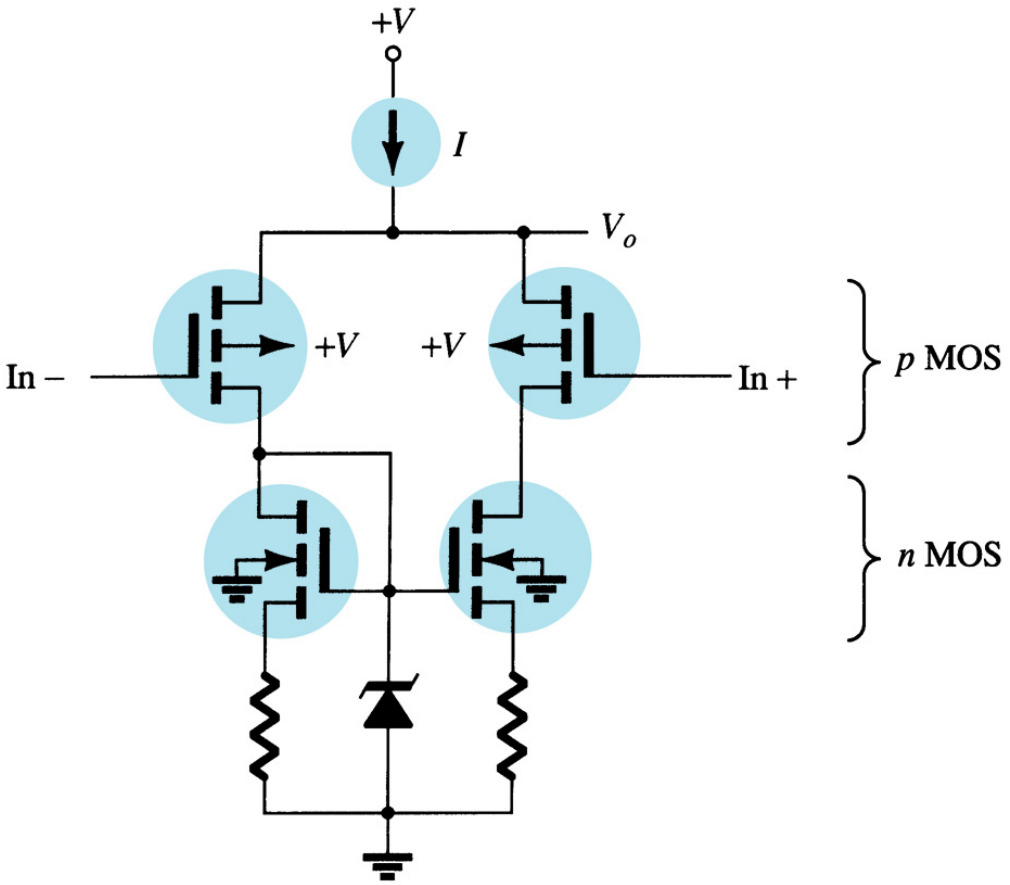
BIMOS Differential Amplifier Circuit

Using MOSFETs as input transistors and BJTs as current sources can further increase the input impedance of the amplifier.



CMOS Differential Amplifier Circuit

A CMOS differential amplifier uses pMOS transistors as input transistors and nMOS transistors as outputs.



A CMOS circuit will have very high input impedance and it will require lower DC source voltages. This makes it well suited for battery-operated devices.

Republic of Iraq

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College of Engineering

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Electronic I

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2018-2019

UNIVERSITY OF ANBAR

COLLEGE OF ENGINEERING

ELECTRICAL ENGINEERING DEPARTMENT

Electronic I

Third Class

Chapter 10

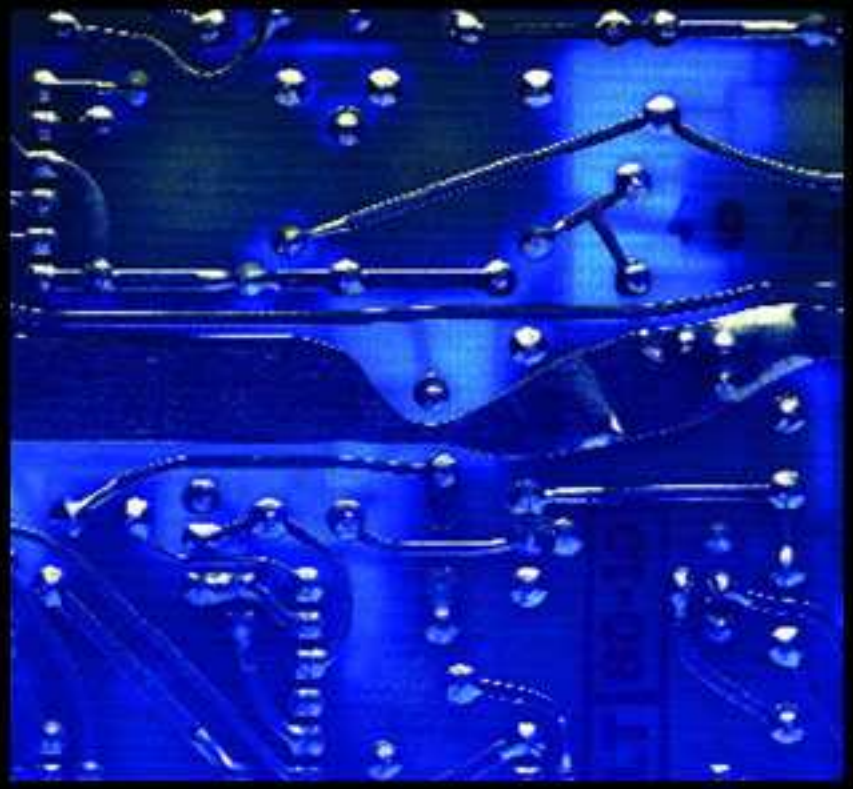
Ch10_ Operational Amplifiers

Hatem Fahd Al-Duliamy

2018-2019

ELECTRONIC DEVICES AND CIRCUIT THEORY

TENTH EDITION



BOYLESTAD

PEARSON

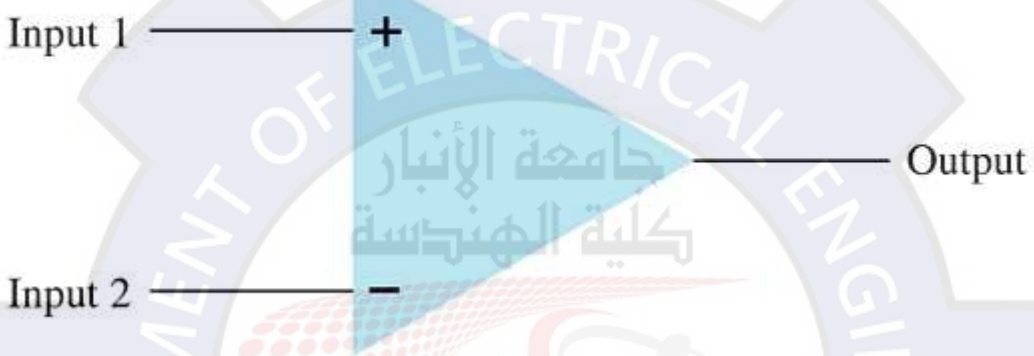
Chapter 10:
Operational Amplifiers

Hatem Fahd Al-Duliamy

CHAPTER OBJECTIVES:

- Understand what a differential amplifier does
- Learn the basics of an operational amplifier
- Develop an understanding of what common mode operation is
- Describe double-ended input operation

Basic Op-Amp



Operational amplifier or op-amp, is a very high gain differential amplifier with a high input impedance (typically a few meg-Ohms) and low output impedance (less than 100 Ω).

Note the op-amp has two inputs and one output.

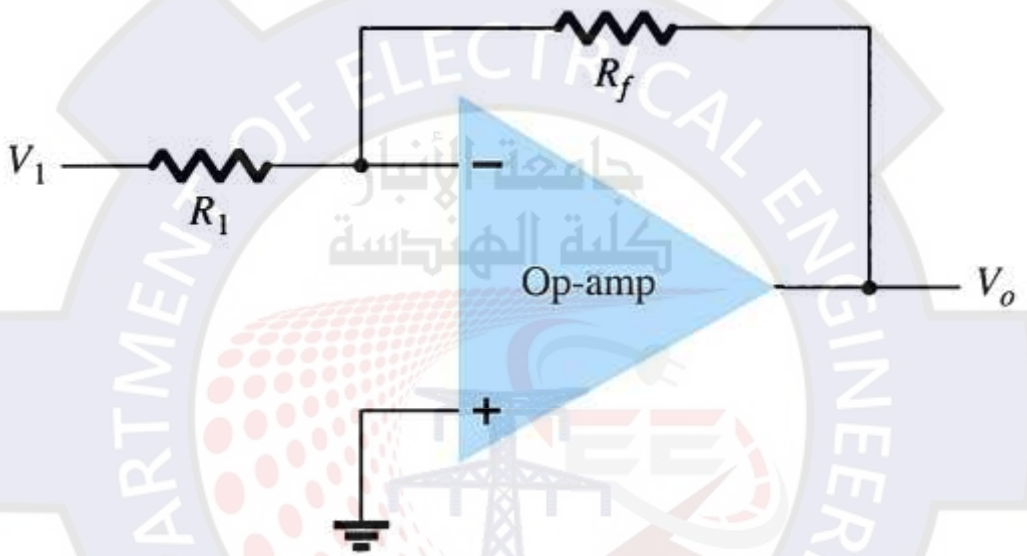
Op-Amp Gain

Op-Amps have a very high gain. They can be connected open-loop or closed-loop.

- **Open-loop refers to a configuration where there is no feedback from output back to the input. In the open-loop configuration the gain can exceed 10,000.**

- **Closed-loop configuration reduces the gain. In order to control the gain of an op-amp it must have feedback. This feedback is a negative feedback. A negative feedback reduces the gain and improves many characteristics of the op-amp.**

Inverting Op-Amp



- The signal input is applied to the inverting (–) input
- The non-inverting input (+) is grounded
- The resistor R_f is the feedback resistor. It is connected from the output to the negative (inverting) input. This is *negative feedback*.

Inverting Op-Amp Gain

Gain can be determined from external resistors: R_f and R_1

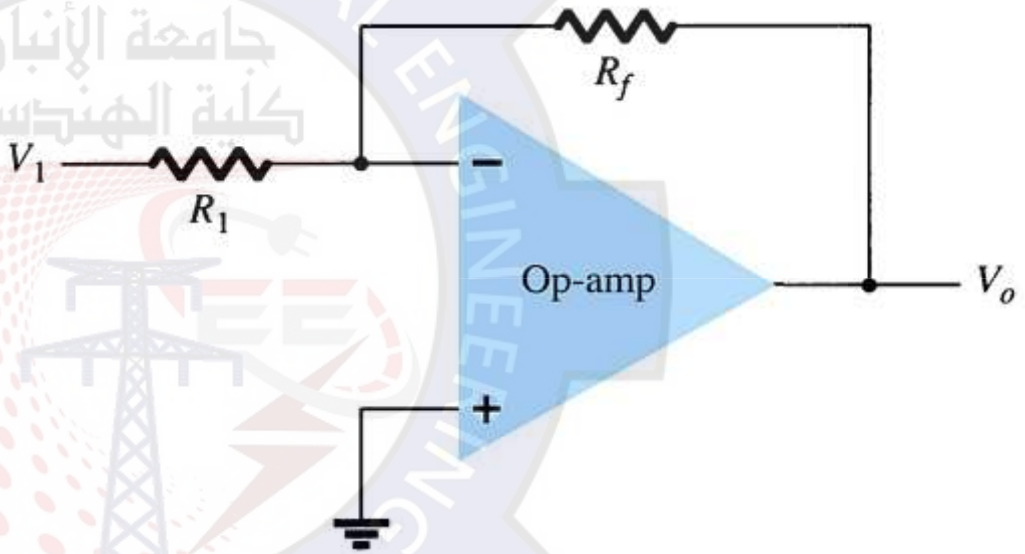
$$A_v = \frac{V_o}{V_i} = \frac{R_f}{R_1}$$

Unity gain—voltage gain is 1

$$R_f = R_1$$

$$A_v = \frac{-R_f}{R_1} = -1$$

The negative sign denotes a 180° phase shift between input and output.

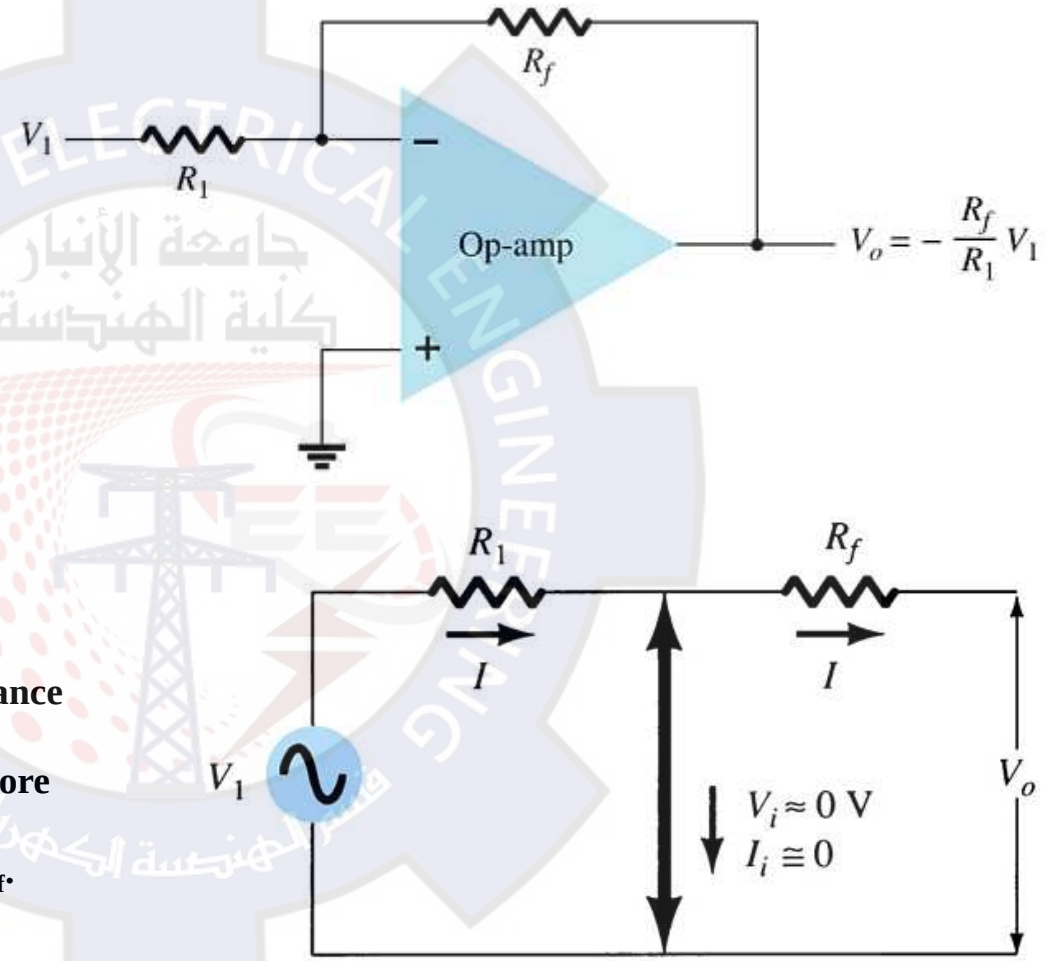


Constant Gain—R_f is a multiple of R_1

Virtual Ground

An understanding of the concept of virtual ground provides a better understanding of how an op-amp operates.

The *non-inverting* input pin is at ground. *The inverting* input pin is also at 0 V for an AC signal.



The op-amp has such high input impedance that even with a high gain there is no current from inverting input pin, therefore there is no voltage from inverting pin to ground—all of the current is through R_f.

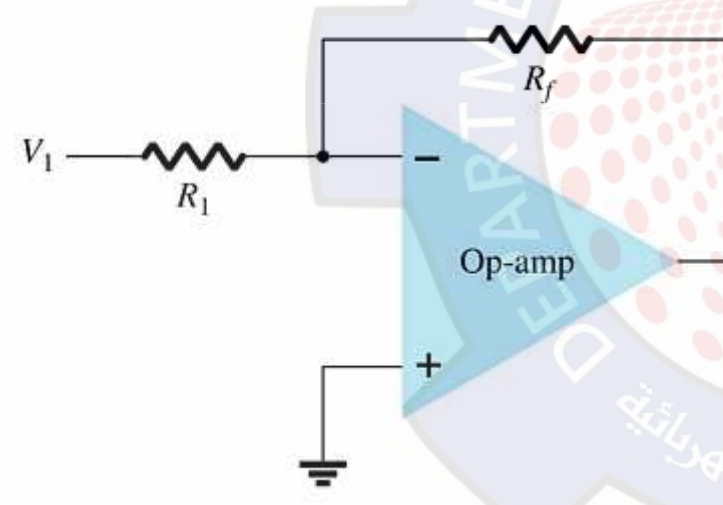
Practical Op-Amp Circuits

Inverting amplifier
Noninverting amplifier
Unity follower
Summing amplifier
Integrator
Differentiator

Inverting/Noninverting Op-Amps

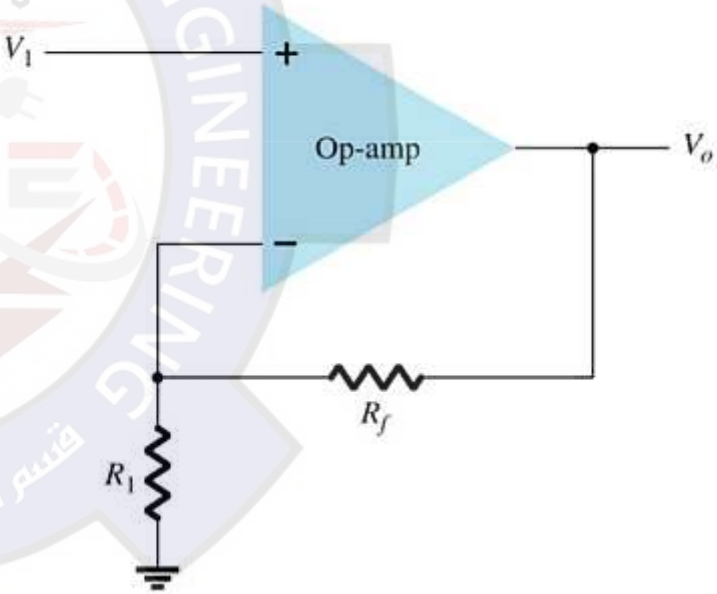
Inverting Amplifier

$$V_o = \frac{-R_f}{R_1} V_1$$



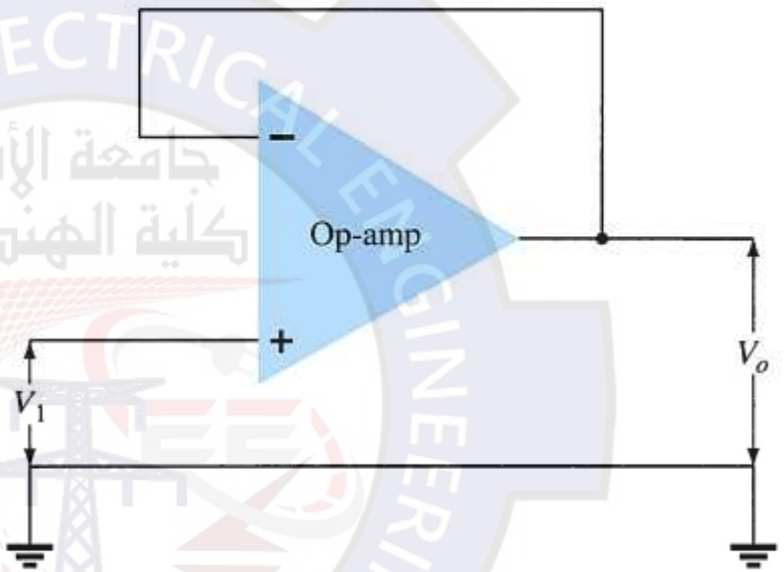
Noninverting Amplifier

$$V_o = \left(1 + \frac{R_f}{R_1}\right) V_1$$



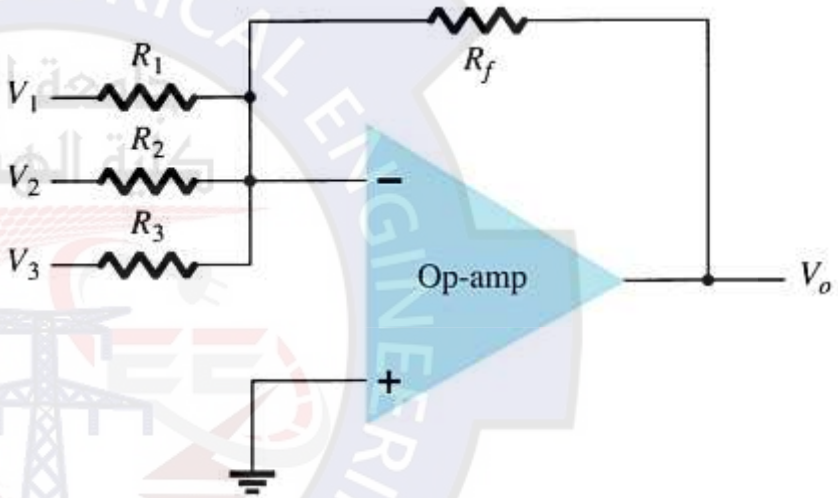
Unity Follower

$$V_o = V_1$$



Summing Amplifier

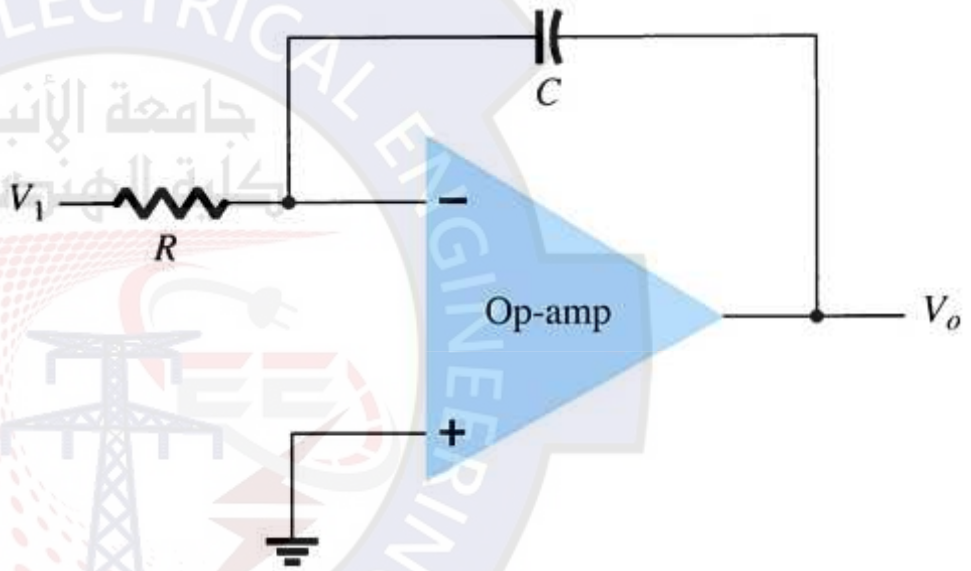
Because the op-amp has a high input impedance, the multiple inputs are treated as separate inputs.



$$V_o = -\left(\frac{R_f}{R_1}V_1 + \frac{R_f}{R_2}V_2 + \frac{R_f}{R_3}V_3\right)$$

Integrator

The output is the integral of the input. Integration is the operation of summing the area under a waveform or curve over a period of time. This circuit is useful in low-pass filter circuits and sensor conditioning circuits.

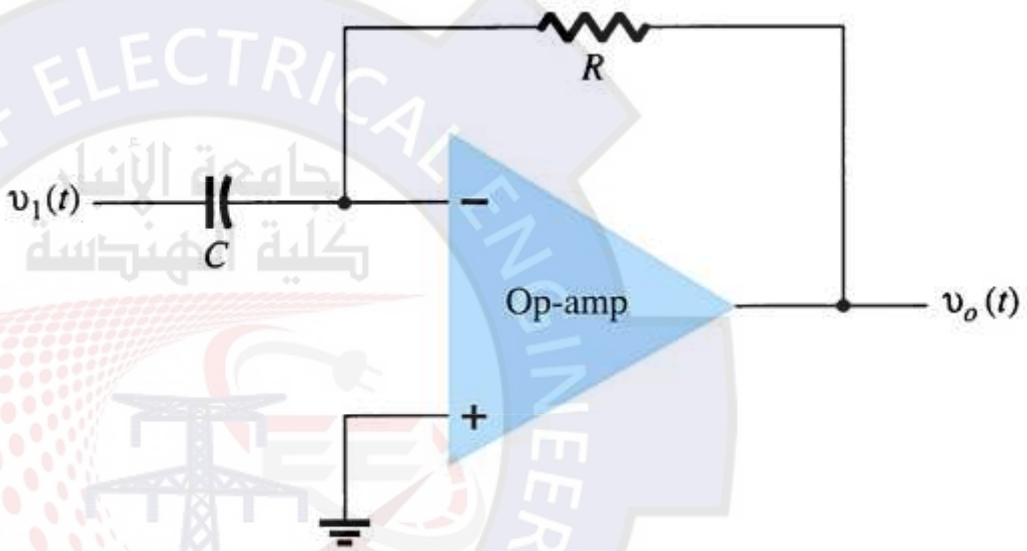


$$v_o(t) = -\frac{1}{RC}\int v_1(t)dt$$

Differentiator

The differentiator takes the derivative of the input. This circuit is useful in high-pass filter circuits.

$$v_o(t) = -RC\frac{dv_1(t)}{dt}$$



Op-Amp Specifications—DC Offset Parameters

Even when the input voltage is zero, there can be an output offset. The following can cause this offset:

- Input offset voltage
- Input offset current
- Input offset voltage *and* input offset current
- Input bias current

Input Offset Voltage (V_{IO})

The specification sheet for an op-amp indicate an input offset voltage (V_{IO}).

The effect of this input offset voltage on the output can be calculated with

$$V_{o(offset)} = V_{IO}\frac{R_1 + R_f}{R_1}$$

Output Offset Voltage Due to Input Offset Current (I_{IO})

If there is a difference between the dc bias currents for the same applied input, then this also causes an output offset voltage:

- The input offset Current (I_{IO}) is specified in the specifications for the op-amp.
- The effect on the output can be calculated using:

$$V_{o(\text{offset due to } I_{IO})} = I_{IO} R_f$$

Total Offset Due to V_{IO} and I_{IO}

Op-amps may have an output offset voltage due to both factors V_{IO} and I_{IO}. The total output offset voltage will be the sum of the effects of both:

$$V_o(\text{offset}) = V_o(\text{offset due to } V_{IO}) + V_o(\text{offset due to } I_{IO})$$

Input Bias Current (I_{IB})

A parameter that is related to input offset current (I_{IO}) is called input bias current (I_{IB})

The separate input bias currents are:

$$I_{IB}^{-} = I_{IB} - \frac{I_{IO}}{2} \qquad I_{IB}^{+} = I_{IB} + \frac{I_{IO}}{2}$$

The total input bias current is the average:

$$I_{IB} = \frac{I_{IB}^{-} + I_{IB}^{+}}{2}$$

Frequency Parameters

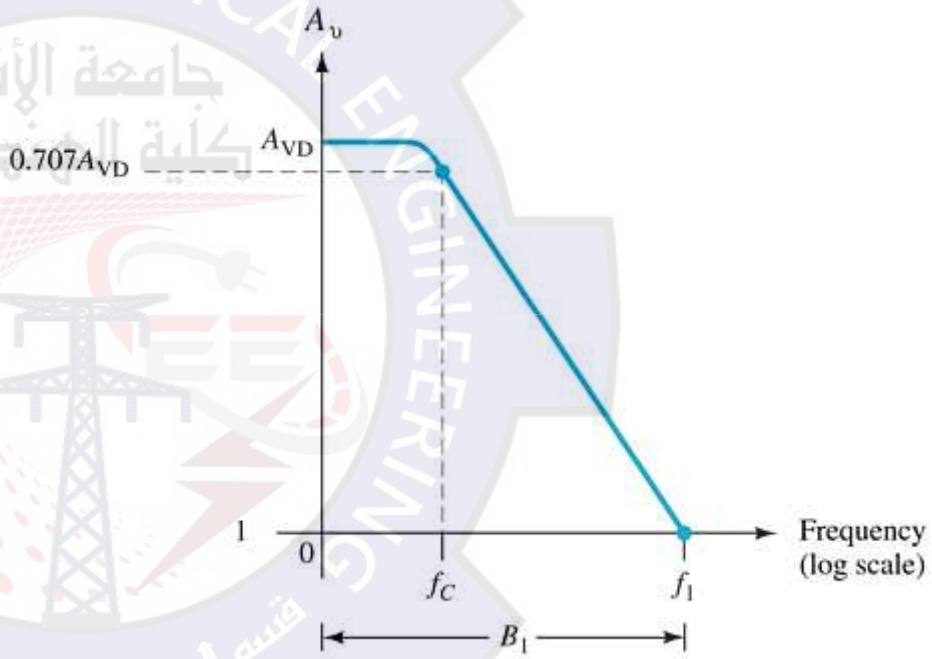
An op-amp is a wide-bandwidth amplifier. The following affect the bandwidth of the op-amp:

- **Gain**
- **Slew rate**

Gain and Bandwidth

The op-amp's high frequency response is limited by internal circuitry. The plot shown is for an open loop gain (A_{OL} or A_{VD}). This means that the op-amp is operating at the highest possible gain with no feedback resistor.

In the open loop, the op-amp has a narrow bandwidth. The bandwidth widens in closed-loop operation, but then the gain is lower.



Slew Rate (SR)

Slew rate (SR) is the maximum rate at which an op-amp can change output without distortion.

$$SR = \frac{\Delta V_o}{\Delta t} \quad \text{(in V/}\mu\text{s)}$$

The SR rating is given in the specification sheets as V/μs rating.

Maximum Signal Frequency

The slew rate determines the highest frequency of the op-amp without distortion.

$$f \leq \frac{SR}{2\pi V_p}$$

where V_P is the peak voltage

General Op-Amp Specifications

Other ratings for op-amp found on specification sheets are:

- **Absolute Ratings**
- **Electrical Characteristics**
- **Performance**

Absolute Ratings

These are common maximum ratings for the op-amp.

Absolute Maximum Ratings	
Supply voltage	6 22 V
Internal power dissipation	500 mW
Differential input voltage	6 30 V
Input voltage	6 15 V

Electrical Characteristics

TABLE 13.2 mA741 Electrical Characteristics: $V_{CC} = \pm 15$ V, $T_A = 25°C$

Characteristic	*MIN*	*TYP*	*MAX*	*Unit*
V_{IO} Input offset voltage		1	6	mV
I_{IO} Input offset current		20	200	nA
I_{IB} Input bias current		80	500	nA
V_{ICR} Common-mode input voltage range	±12	±13		V
V_{OM} Maximum peak output voltage swing	±12	±14		V
A_{VD} Large-signal differential voltage amplification	20	200		V/mV
r_i Input resistance	0.3	2		MΩ
r_o Output resistance		75		Ω
C_i Input capacitance		1.4		pF
CMRR Common-mode rejection ratio	70	90		dB
I_{CC} Supply current		1.7	2.8	mA
P_D Total power dissipation		50	85	mW

Note: These ratings are for specific circuit conditions, and they often include minimum, maximum and typical values.

CMRR

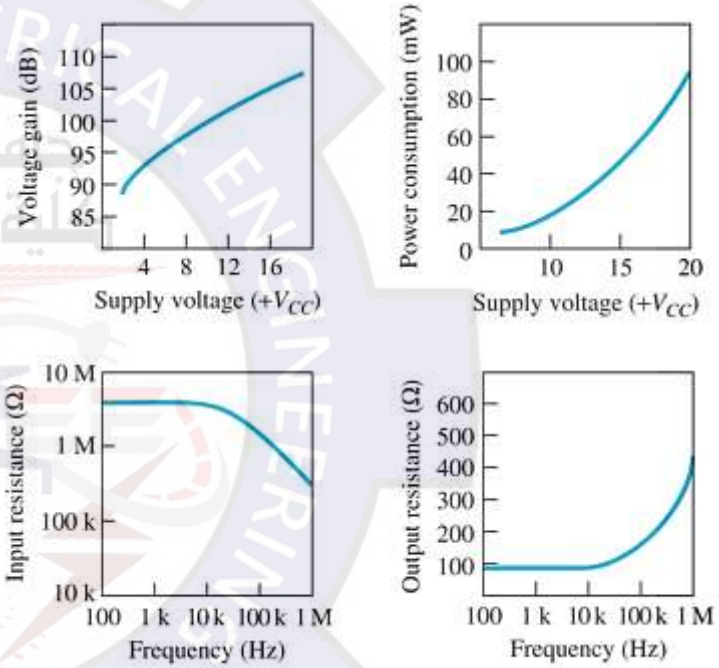
One rating that is unique to op-amps is CMRR or common-mode rejection ratio.

Because the op-amp has two inputs that are opposite in phase (inverting input and the non-inverting input) any signal that is common to both inputs will be cancelled.

Op-amp CMRR is a measure of the ability to cancel out common-mode signals.

Op-Amp Performance

The specification sheets will also include graphs that indicate the performance of the op-amp over a wide range of conditions.



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College of Engineering

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Electronic I

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2018-2019

UNIVERSITY OF ANBAR

COLLEGE OF ENGINEERING

ELECTRICAL ENGINEERING DEPARTMENT

Electronic I

Third Class

Chapter 11

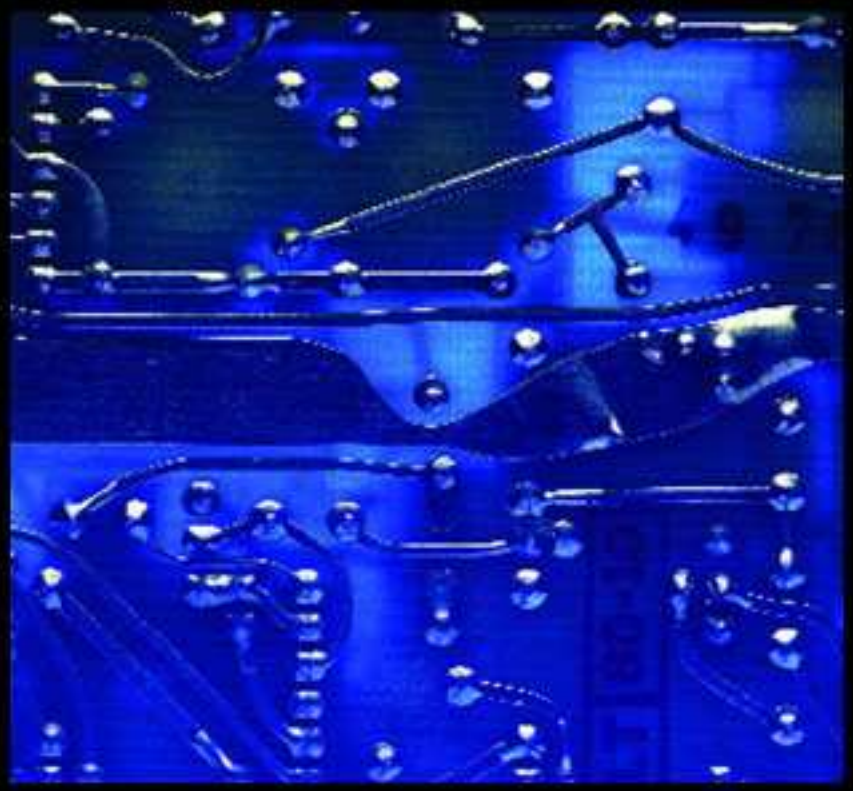
Ch11_ Operational Amplifiers Applications

Hatem Fahd Al-Duliamy

2018-2019

ELECTRONIC DEVICES AND CIRCUIT THEORY

TENTH EDITION



BOYLESTAD

PEARSON

Chapter 11: Operational Amplifiers Applications

Hatem Fahd Al-Duliamy

CHAPTER OBJECTIVES:

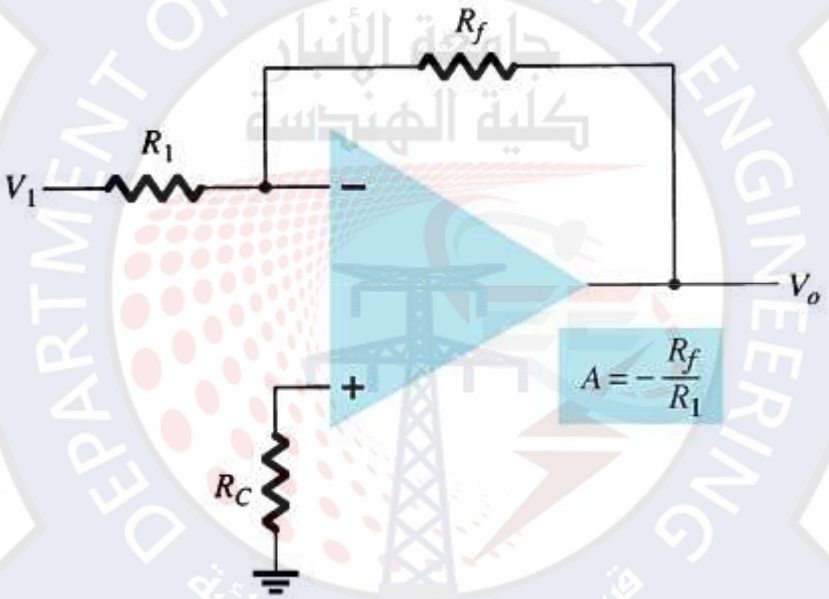
- Learn about constant gain, summing, and buffering amplifiers
- Understand how an active filter works
- Describe different types of controlled sources

Op-Amp Applications

Constant-gain multiplier
Voltage summing
Voltage buffer
Controlled sources
Instrumentation circuits
Active filters

Constant-Gain Amplifier

Inverting Version



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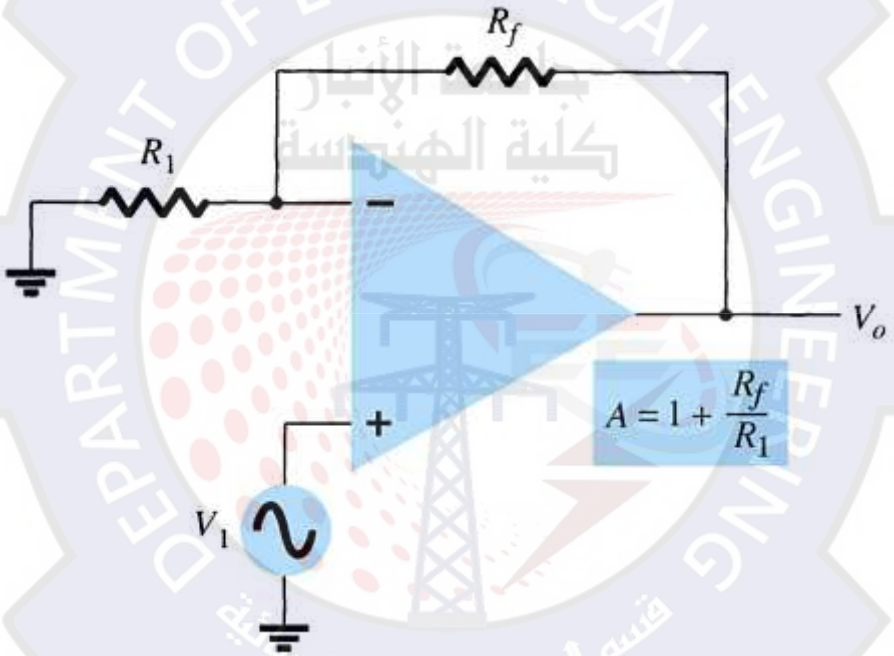
Constant-Gain Amplifier

Noninverting Version



Multiple-Stage Gains

The total gain (3-stages) is given by:

$$A = A_1 A_2 A_3$$

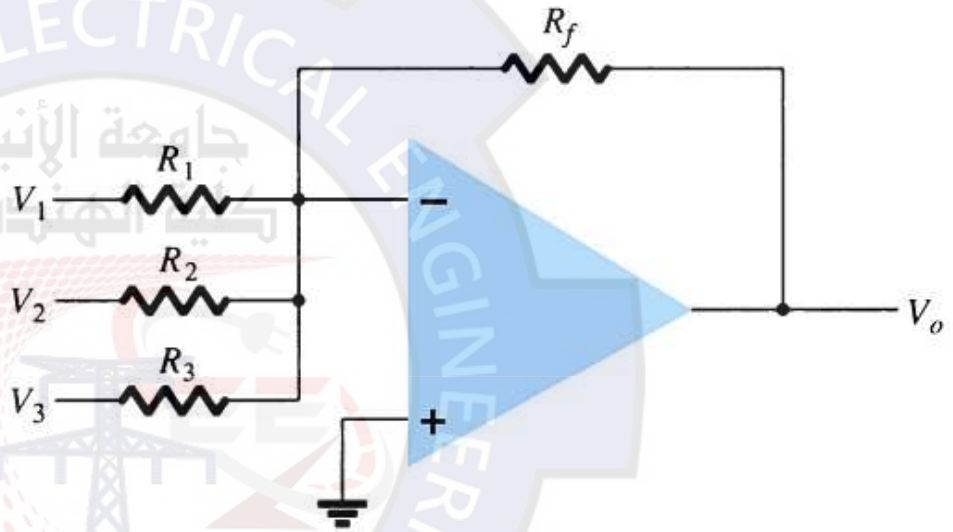
or

$$A = \left(1 + \frac{R_f}{R_1}\right)\left(-\frac{R_f}{R2}\right)\left(-\frac{R_f}{R3}\right)$$

Voltage Summing

The output is the sum of individual signals times the gain:

$$V_o = -\left(\frac{R_f}{R_1}V_1 + \frac{R_f}{R_2}V_2 + \frac{R_f}{R_3}V_3\right)$$



[Formula 14.3]

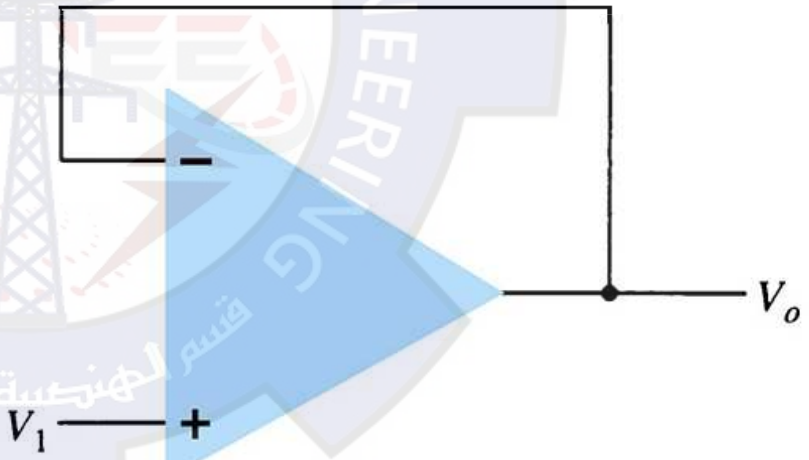
Voltage Buffer

Any amplifier with no gain or loss is called a unity gain amplifier.

The advantages of using a unity gain amplifier:

- **Very high input impedance**
- **Very low output impedance**

Realistically these circuits are designed using equal resistors ($R_1 = R_f$) to avoid problems with offset voltages.



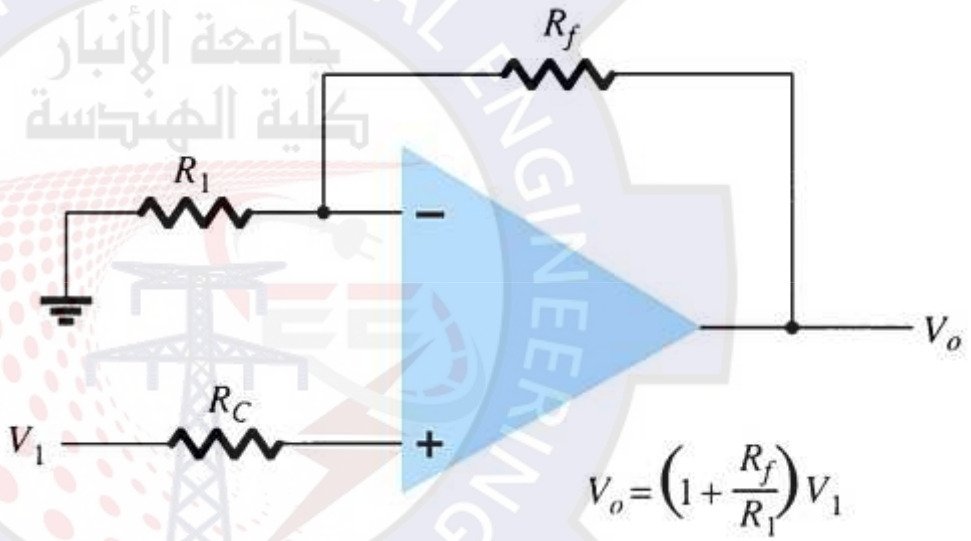
Controlled Sources

Voltage-controlled voltage source
Voltage-controlled current source
Current-controlled voltage source
Current-controlled current source

Voltage-Controlled Voltage Source

The output voltage is the gain times the input voltage. What makes an op-amp different from other amplifiers is its impedance characteristics and gain calculations that depend solely on external resistors.

Noninverting Amplifier Version

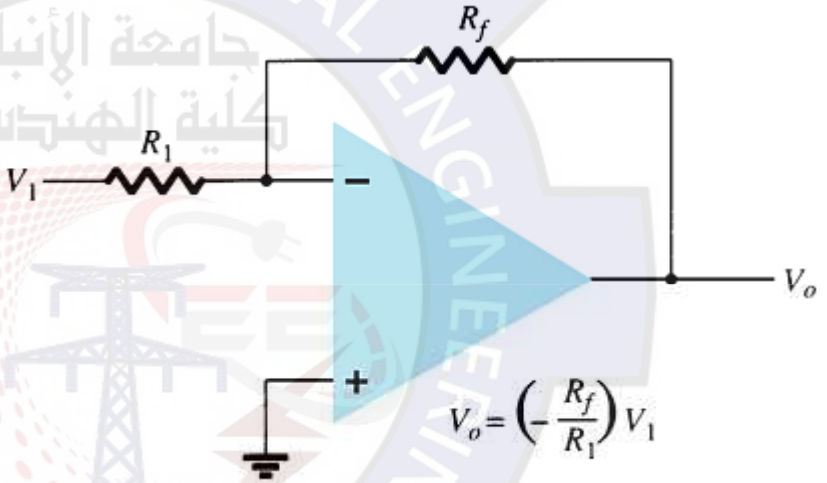


more…

Voltage-Controlled Voltage Source

The output voltage is the gain times the input voltage. What makes an op-amp different from other amplifiers is its impedance characteristics and gain calculations that depend solely on external resistors.

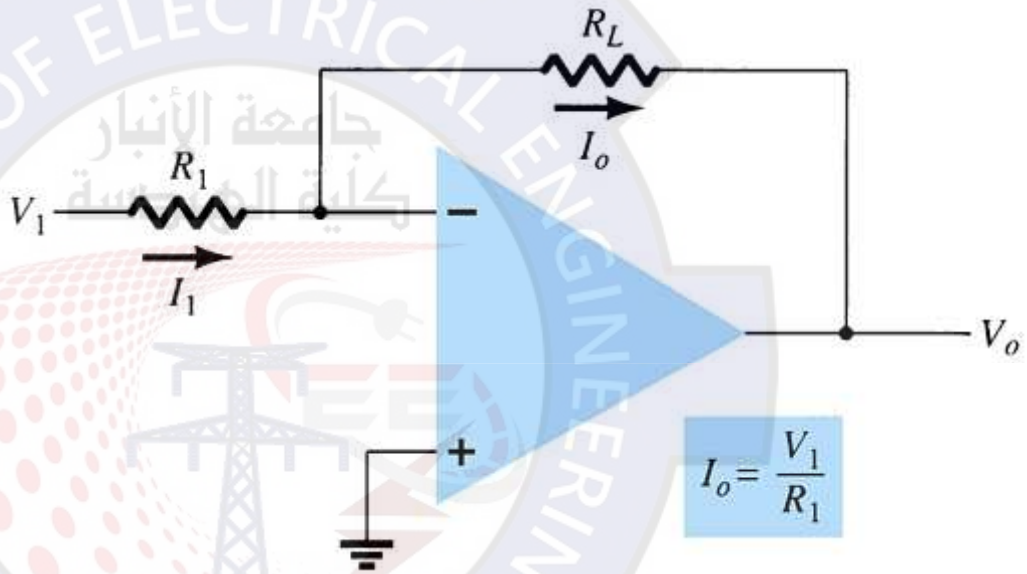
Inverting Amplifier Version



Voltage-Controlled Current Source

The output current is:

$$I_o = \frac{V_1}{R_1} = kV_1$$



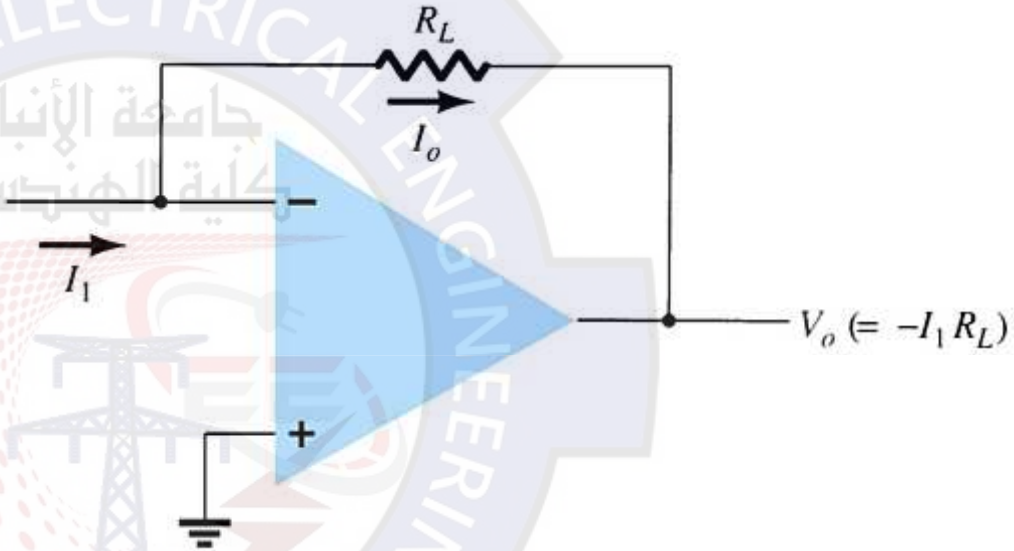
Current-Controlled Voltage Source

This is simply another way of applying the op-amp operation. Whether the input is a current determined by V_{in}/R_1 or as I_1:

$$V_{out} = \frac{-R_f}{R_1} V_{in}$$

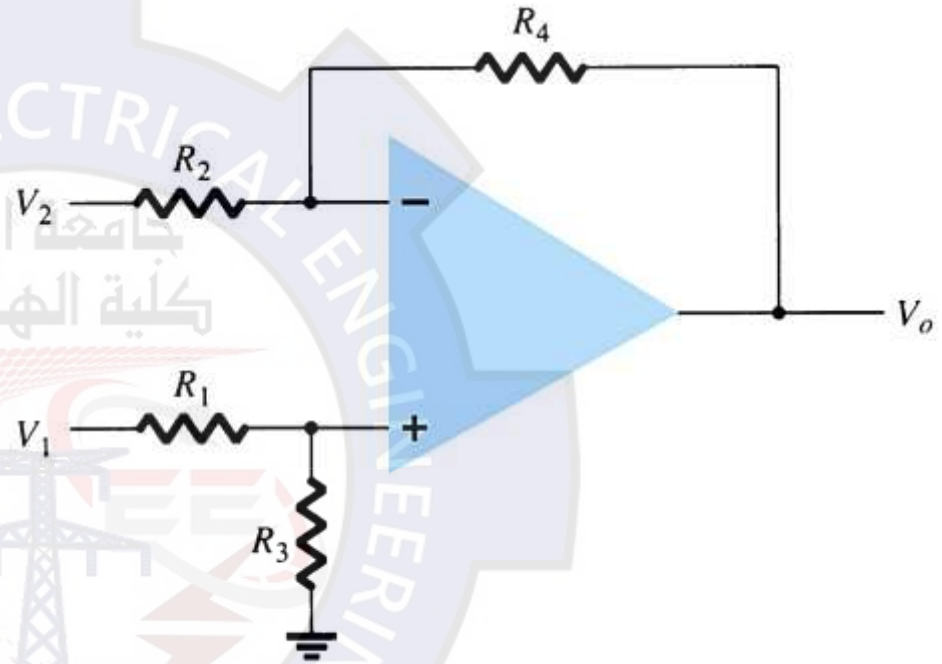
or

$$V_{out} = -I_1 R_L$$



Current-Controlled Current Source

This circuit may appear more complicated than the others but it is really the same thing.



$$V_{out} = -\left(\frac{R_f}{R_{in}}\right)V_{in} \qquad I_o = -\frac{V_{in}}{R_1 \| R_2}$$

$$\frac{V_{out}}{R_f} = -\frac{V_{in}}{R_1 \| R_2} \qquad I_o = -V_{in}\left(\frac{R_1 + R_2}{R_1 \times R_2}\right)$$

$$\frac{V_{out}}{R_f} = -\frac{V_{in}}{R_{in}} \qquad I_o = -\frac{V_{in}}{R_1}\left(\frac{R_1 + R_2}{R_2}\right)$$

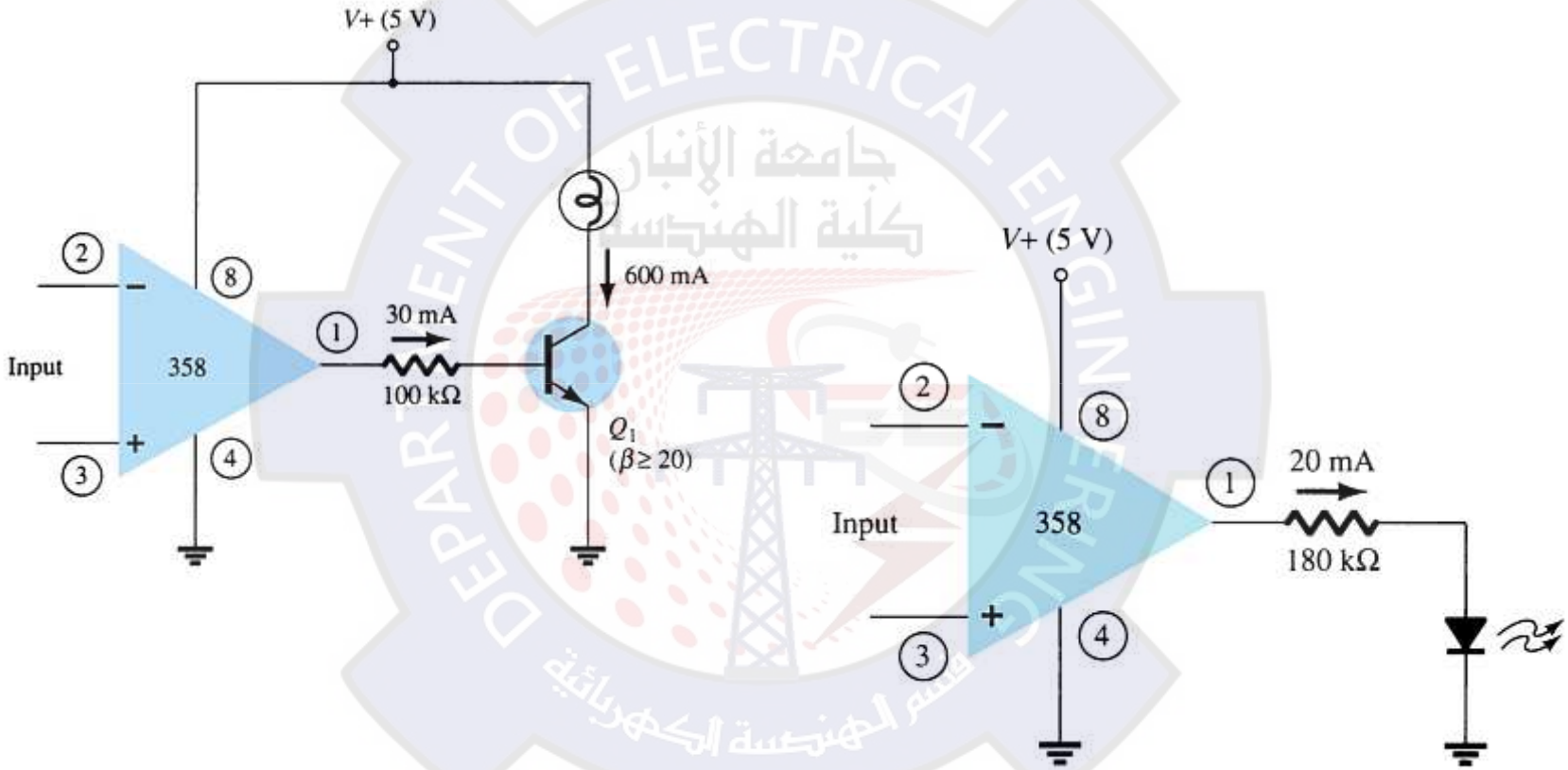
$$I_o = -I\left(1 + \frac{R_1}{R_2}\right) = kI$$

Instrumentation Circuits

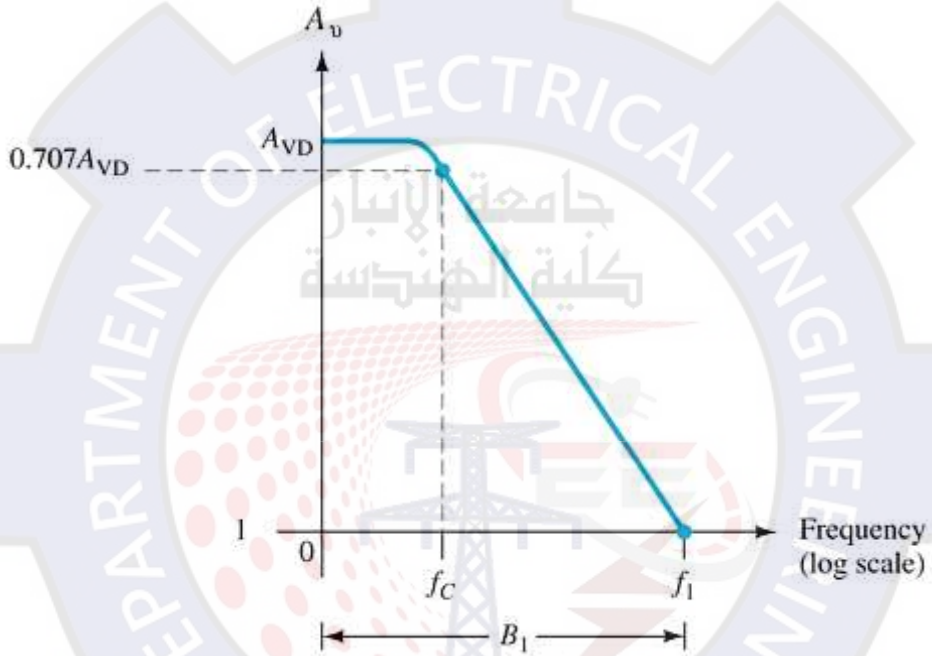
Some examples of instrumentation circuits using op-amps:

- **Display driver**
- **Instrumentation amplifier**

Display Driver



Instrumentation Amplifier



For all Rs at the same value (except R_p):

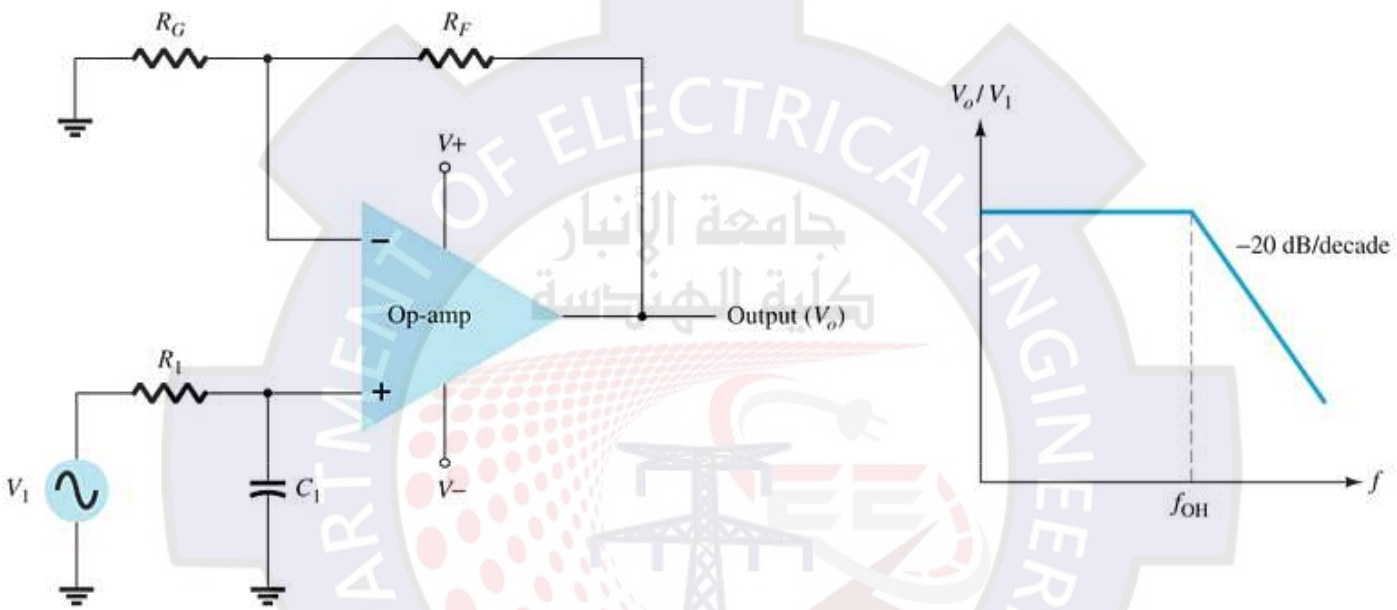
$$V_o = \left(1 + \frac{2R}{R_P}\right)(V_1 - V_2) = k(V_1 - V_2)$$

Active Filters

Adding capacitors to op-amp circuits provides external control of the cutoff frequencies. The op-amp active filter provides controllable cutoff frequencies and controllable gain.

- **Low-pass filter**
- **High-pass filter**
- **Bandpass filter**

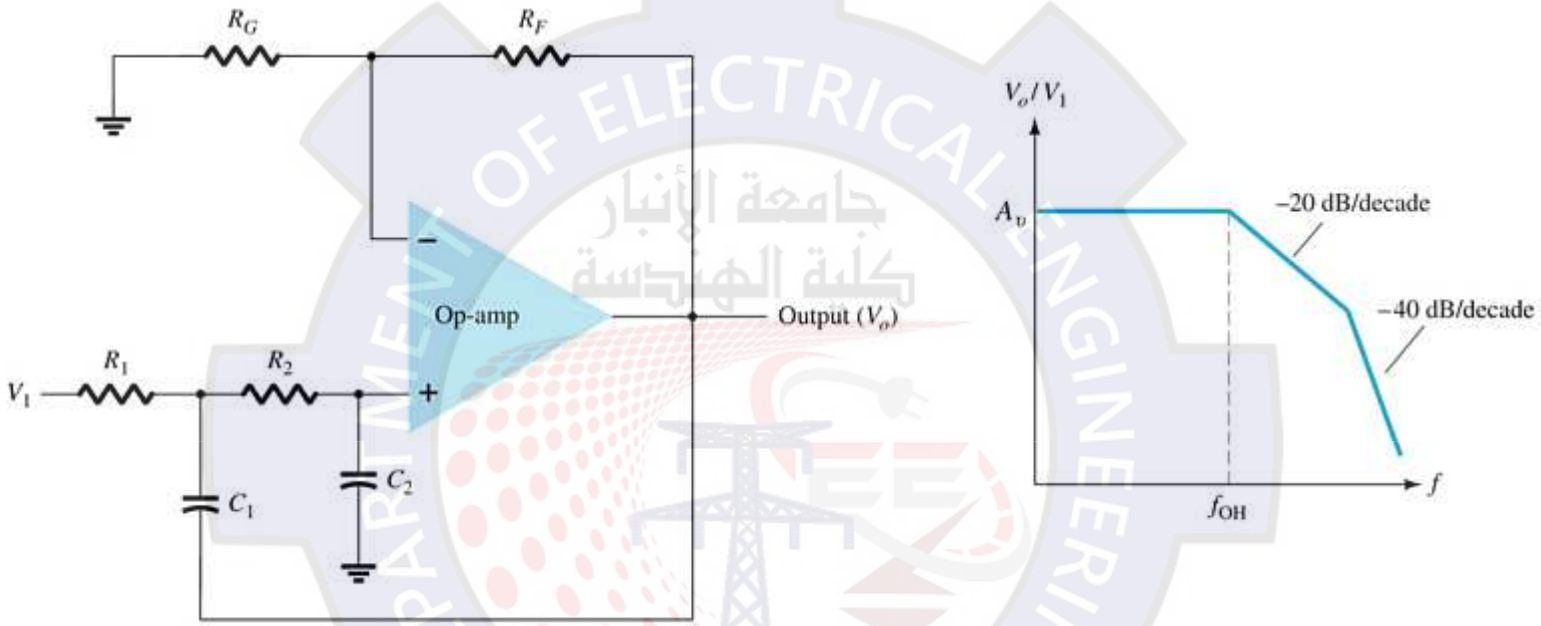
Low-Pass Filter—First-Order



The upper cutoff frequency and voltage gain are given by:

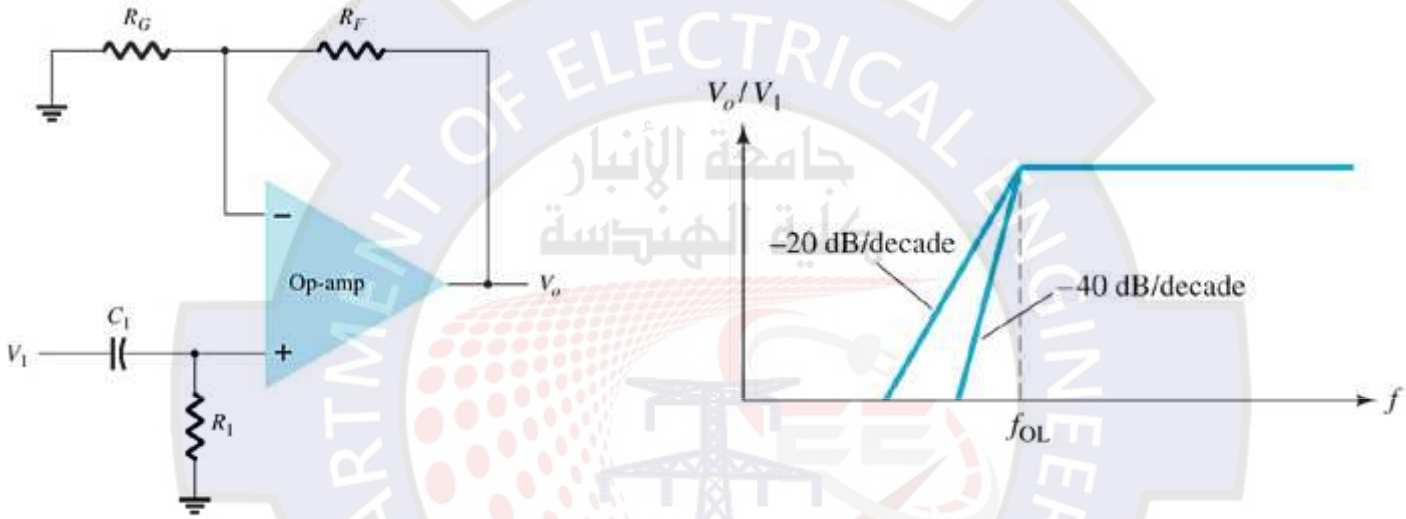
$$f_{OH} = \frac{1}{2\pi R_1 C_1} \qquad A_v = 1 + \frac{R_f}{R_1}$$

Low-Pass Filter—Second-Order



The roll-off can be made steeper by adding more RC networks.

High-Pass Filter



The cutoff frequency is determined by:

$$f_{OL} = \frac{1}{2\pi R_1 C_1}$$

Bandpass Filter

There are two cutoff frequencies: upper and lower. They can be calculated using the same low-pass cutoff and high-pass cutoff frequency formulas in the appropriate sections.